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CONTROL DATA CORPORATION

CDC® CYBER 170 MODELS 720, 730, 740, 750 AND 760 MODEL 176 (LEVEL B/C) COMPUTER SYSTEMS

CODES

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REVISION RECORD

Revision	Description
A (06-09-80)	Manual released.
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New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot in the lower right corner if the entire frame is affected.

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LIST OF EFFECTIVE PAGES

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PREFACE

This codes booklet contains code and timing information for the CDC® CYBER 170 Computer Systems, Models 720, 730, 740, 750, 760, and 176 (Level B/C). For model 176, level B is equivalent to any of the model designators 408 through 444; level C is model designator 501.

NOTE

Refer to publication number 60420010 for codes information on models 171 through 175 and model 176 (level A). For model 176, level A is equivalent to any of the model designators 8 through 44.

The information in this booklet is from the hardware reference manuals listed below. This information does not supplant nor is it as complete as the information contained in the reference manuals. The reference manuals are, at all times, more authoritative, reliable, and current than the codes booklet.

Control Data Publication	Publication Number
CYBER Models 720, 730, 740, 750 and 760 Model 176 (Level B/C) Reference Manual	60456100
7030-1XX ECS II and 6642-2 Distributive Data Path Hardware Reference Manual	60430000
CYBER 70 Computer Systems 7030 Extended Core Storage Reference Manual, Volume 3	60347100
CC545-C/D/E/F Display Station Hardware Reference/Customer Engineering Manual	62952600

Refer to Control Data's Literature and Distribution Services catalog for the latest manual revision levels and literature ordering procedures.

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TABLES

CENTRAL PROCESSOR INSTRUCTIONS 1

This segment of the manual describes the central processor (CP) instructions. Some differences exist in the CP instructions because of model differences. The instruction differences are identified with the applicable model numbers.

INSTRUCTION FORMATS

Program instruction words are divided into four 15-bit fields called parcels. The first parcel (parcel 0) is the highest-order 15 bits of the 60-bit word. The second, third, and fourth parcels (parcels 1, 2, and 3) follow in order. An instruction may occupy one, two, or four parcels, depending on the type of instruction. When an instruction occupies two parcels, it must occupy two parcels within the same program word. Possible parcel arrangements are illustrated in figure 1-1. Instruction designators are listed and defined in table 1-1.

A program word may be filled with a one-parcel pass instruction or an instruction acting as a two-parcel pass instruction. These instructions are used to fill a program word when necessary to place a particular instruction in the first parcel of a program word or to avoid starting a two-parcel instruction in the fourth parcel of a program word. Pass instructions may also be used for branch entry points because a branch instruction destination address must begin with a new word. One-parcel instructions are 460xx through 463xx. Instructions 60xxx through 62xxx may be used as two-parcel pass instructions by setting the i instruction designator to zero.

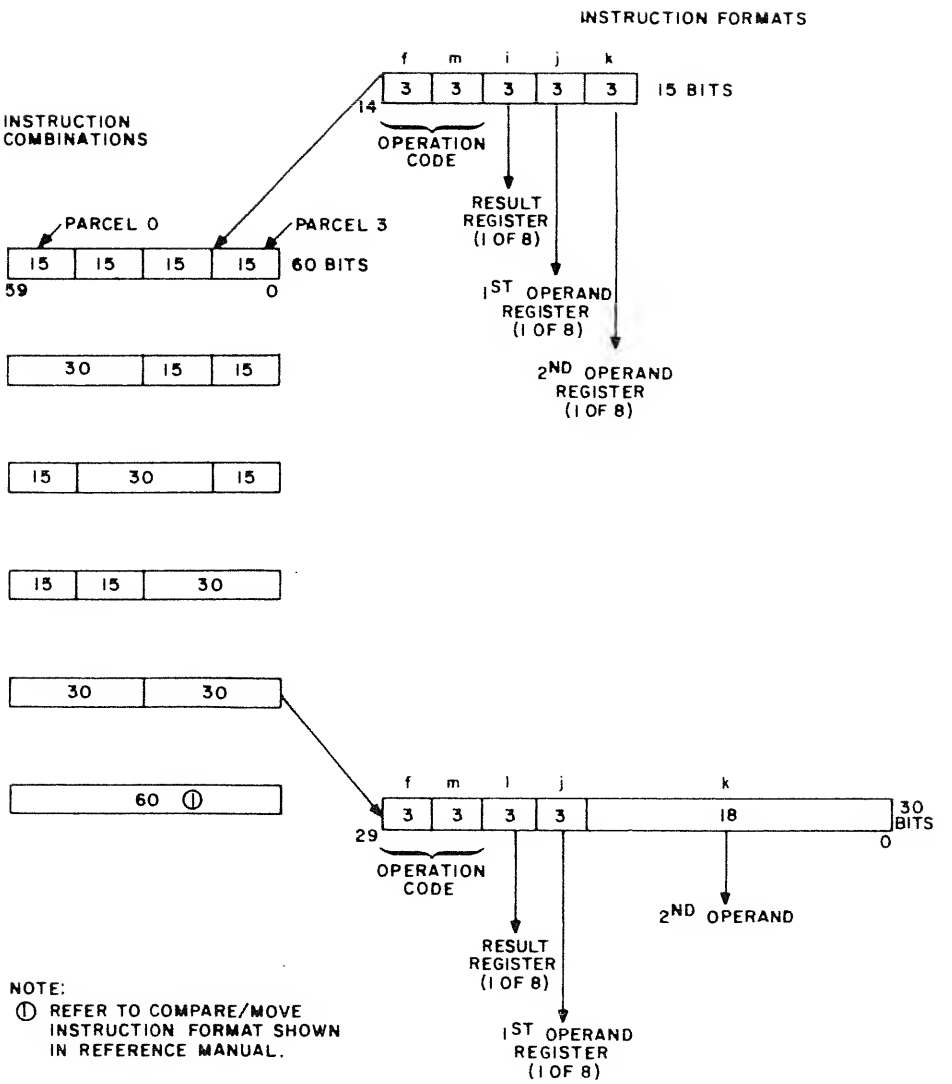

Figure 1-1. CP Instruction Formats

TABLE 1-1. CP INSTRUCTION DESIGNATORS

Designator	Use
fm	6-bit instruction code.
fmi	9-bit instruction code.
i	3-bit code specifying one of eight registers.
j	3-bit code specifying one of eight registers.
jk	6-bit code specifying amount of shift or mask.
k	3-bit code specifying one of eight registers.
K	18-bit operand or address.
x	Unused designator.
A	One of eight 18-bit address registers.
B	One of eight 18-bit index registers; B0 is fixed and equal to zero.
X	One of eight 60-bit operand registers.
( )	Content of a register or location.
Compare/Move (Models 720 and 730)	
C1	Offset (character address) of the first character in the first word of the source field.
C2	Character address of the first character in the first word of the result field.
K1	18-bit address indicating the central memory location of the first (leftmost) character of the source field.

TABLE 1-1. CP INSTRUCTION DESIGNATORS (Contd)

Designator	Use
K2	18-bit address indicating the central memory location of the first (leftmost) character of the result field.
LL	Lower 4 bits of the field length (character count) for a move/compare instruction; used with LU to specify field length.
LU	Upper 9 bits of the field length (character count) for indirect move instruction or the upper 3 bits for direct instructions; used with LL to specify field length.

EXIT MODE

NOTE

Exit mode applies only to models 720 through 760.

UNCONDITIONAL

If the error is an illegal instruction, breakpoint, or an address-range error on an RNI or branch, the program interruption is unconditional.

SELECTED

Mode selection bits determine program interruption for certain error conditions. If a mode selection bit is set and the corresponding exit error condition is detected, the program is interrupted. Exit condition and mode selection bits and the error condition bits set in RAC are as follows:

Exit Condition Bit	Mode Selection Bit	Error Condition
48	48	Address range error.
49	49	Infinite mode.
50	50	Indefinite mode.
51	57	Parity error on ECS flag register operation.
52	58	CPU to CMC address or data parity error or CPU to CM address parity error.
53	59	CMC to CPU data parity error or double error.

Figure 1-2 shows the format of relative address zero on an error exit.

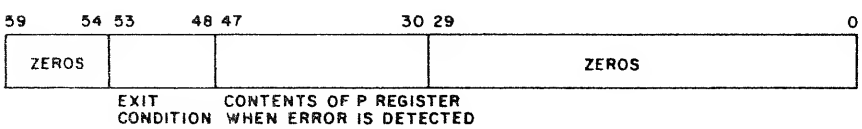

Figure 1-2. Relative Address Zero on Error Exit

CP INSTRUCTIONS AND EXECUTION TIMES

The CP instructions and their execution times appear in tables as follows:

Models 720 and 730 (tables 1-2 and 1-3).

Models 740, 750, and 760 (tables 1-4 and 1-5).

Model 176 (tables 1-6 and 1-7).

For each model, the first table listed contains the CP instructions in numeric sequence. The second table listed contains the CP instructions in functional groups. All of the tables list the instruction execution times based on no conflicts. The execution times are in clock periods which differ according to the model as follows:

Models 720 and 730, 50-nanosecond clock period.

Models 740, 750, and 760, 25-nanosecond clock period.

Model 176, 27.5-nanosecond clock period.

TABLE 1-2. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 AND 730

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
00xxx	Error exit to MA or program stop	-	-	2
010xK	Return jump to K	32 (CP-0) 36 (CP-1)	25 (CP-0) 25 (CP-1)	-
011jK	Block copy (Bj) + K words from ECS to CM	2[(BJ)+K]	2[(BJ)+K]	3
012jK	Block copy (Bj) + K words from CM to ECS	2[(BJ)+K]	2[(BJ)+K]	3
013jK	Central exchange jump to (Bj) + K (monitor flag set)	45	45	-
013xx	Central exchange jump to MA (monitor flag not set)	45	45	-
02ixK	Jump to (Bi) + K	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
030jK	Branch to K if (Xj) = 0	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
031jK	Branch to K if (Xj) ≠ 0	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
032jK	Branch to K if (Xj) positive	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
033jK	Branch to K if (Xj) negative	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
034jK	Branch to K if (Xj) in range	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
035jK	Branch to K if (Xj) out of range	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
036jK	Branch to K if (Xj) definite	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
037jK	Branch to K if (Xj) indefinite	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
04ijK	Branch to K if (Bi) = (Bj)	27 (CP-0) 29 (CP-1)	20 (CP-0) 21 (CP-1)	4
05ijK	Branch to K if (Bi) ≠ (Bj)	27 (CP-0) 29 (CP-1)	20 (CP-0) 21 (CP-1)	4

TABLE 1-2. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 AND 730 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
06ijK	Branch to K if (Bi) $\geq$ (Bj)	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
07ijK	Branch to K if (Bi) < (Bj)	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
10ijx	Transmit (Xj) to Xi	10	3	-
11ijk	Logical product of (Xj) and (Xk) to Xi	12	5	-
12ijk	Logical sum of (Xj) and (Xk) to Xi	12	5	-
13ijk	Logical difference of (Xj) and (Xk) to Xi	12	5	-
14ixk	Transmit complement of (Xk) to Xi	10	3	-
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	12	5	-
16ijk	Logical sum of (Xj) and complement of (Xk) to Xi	12	5	-
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	12	5	-
20ijk	Left shift (Xi) by jk	12	5	-
21ijk	Right shift (Xi) by jk		12	5
22ijk	Left shift (Xk) nominally (Bj) places to Xi	12	5	-
23ijk	Right shift (Xk) nominally (Bj) places to Xi	12	5	-
24ijk	Normalize (Xk) to Xi and Bj	13	6	-
25ijk	Round normalize (Xk) to Xi and Bj	13	6	-

TABLE 1-2. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 AND 730 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
26ijk	Unpack (Xk) to Xi and Bj	12	5	-
27ijk	Pack (Xk) and (Bj) to Xi	12	5	-
30ijk	Floating sum of (Xj) and (Xk) to Xi	16	9	-
31ijk	Floating difference of of (Xj) and (Xk) to Xi	16	9	-
32ijk	Floating double-precision sum of (Xj) and (Xk) to Xi	16	9	-
33ijk	Floating double-precision difference of (Xj) and (Xk) to Xi	16	9	-
34ijk	Round floating sum of (Xj) and (Xk) to Xi	16	9	-
35ijk	Round floating difference of (Xj) and (Xk) to Xi	16	9	-
36ijk	Integer sum of (Xj) and (Xk) to Xi	12	5	-
37ijk	Integer difference of (Xj) and (Xk) to Xi	12	5	-
40ijk	Floating product of (Xj) and (Xk) to Xi	63	57	-
41ijk	Round floating product of (Xj) and (Xk) to Xi	63	57	-
42ijk	Floating double-precision product of (Xj) and (Xk) to Xi	63	57	-
43ijk	Form mask of jk bits to Xi	12	5	-
44ijk	Floating divide (Xj) by (Xk) to Xi	63	57	-

TABLE 1-2. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 AND 730 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
45ijk	Round floating divide (Xj) by (Xk) to Xi	63	57	-
460xx	Pass	10	3	-
464jK	Move indirect	-	-	5,6
465	Move direct	-	-	5,7
466	Compare collated	-	-	5,8
467	Compare uncollated	-	-	5,9
47ixk	Population count of (Xk) to Xi	73	67	-
50ijK	Set Ai to (Aj) + K	25	18	10
51ijK	Set Ai to (Bj) + K	25	18	10
52ijK	Set Ai to (Xj) + K	25	18	10
53ijk	Set Ai to (Xj) + (Bk)	25	18	10
54ijk	Set Ai to (Aj) + (Bk)	25	18	10
55ijk	Set Ai to (Aj) - (Bk)	25	18	10
56ijk	Set Ai to (Bj) + (Bk)	25	18	10
57ijk	Set Ai to (Bj) - (Bk)	25	18	10
60ijK	Set Bi to (Aj) + K	11	4	-
61ijK	Set Bi to (Bj) + K	11	4	-
62ijK	Set Bi to (Xj) + K	11	4	-
63ijk	Set Bi to (Xj) + (Bk)	11	4	-
64ijk	Set Bi to (Aj) + (Bk)	11	4	-
65ijk	Set Bi to (Aj) - (Bk)	11	4	-
66ijk	Set Bi to (Bj) + (Bk)	11	4	-
67ijk	Set Bi to (Bj) - (Bk)	11	4	-
70ijK	Set Xi to (Aj) + K	12	5	-

TABLE 1-2. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 AND 730 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
71ijK	Set Xi to (Bj) + K	12	5	-
72ijK	Set Xi to (Xj) + K	12	5	-
73ijk	Set Xi to (Xj) + (Bk)	12	5	-
74ijk	Set Xi to (Aj) + (Bk)	12	5	-
75ijk	Set Xi to (Aj) - (Bk)	12	5	-
76ijk	Set Xi to (Bj) + (Bk)	12	5	-
77ijk	Set Xi to (Bj) - (Bk)	12	5	-

Notes:

1. Instruction placement within a program instruction word may affect the RNI initiation time and the total execution time of the program.

2. When used as error exit, 00 instructions take 52 clock periods.

3. The time does not include startup time and assumes no ECS record gaps.

4. If jump condition is not met, the execution times are: model 720, 12 clock periods and model 730, 5 clock periods.

5. Formulas (given in notes 6 through 9) for instruction execution times give only approximate times. The following assumptions make the formulas useful only as best-case calculations.

   a. No offset in either the source field or the destination field (C1=C2=zero).

   b. No memory conflicts from the rest of the system (PPs, second CP, or ECS).

   c. No conflicts within the instruction.

   d. All words compare for instruction 467.

TABLE 1-2. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 AND 730 (Contd)

NOTE

Formula term explanations for notes 6 through 9 are:

T Time required for instruction execution in nanoseconds.

L Number of characters in the operation.

N Word count, calculated as L/10.

X Number of collate operations which require two memory references.

Y Number of collate operations which require one memory reference.

Z Number of collate operations which do not require memory references.

6. Execution time for models 720 and 730:

For CP-0, T = 900 + execution time for instruction 465.

For CP-1, T = 1000 + execution time for instruction 465.

7. Execution time for model 720:

For CP-0, T = 2000 + 200N, for N = 1 through 4.

For CP-0, T = 1000 + 400N, for N ≥ 5.

For CP-1, T = 2100 + 200N, for N = 1 through 5.

For CP-1, T = 1200 + 400N, for N ≥ 6.

Execution time for model 730:

For CP-0, T = 1650 + 200N, for N = 1 through 4.

For CP-0, T = 650 + 400N, for N ≥ 5.

For CP-1, T = 1750 + 200N, for N = 1 through 5.

For CP-1, T = 850 + 400N, for N ≥ 6.

TABLE 1-2. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 AND 730 (Contd)

8. Execution time for model 720:

For CP-0, T = 1050 + 650N + 1500X + 1250Y + 300Z, if N is even.

For CP-0, T = 1300 + 650N + 1500X + 1250Y + 300Z, if N is odd.

For CP-1, T = 1150 + 700N + 1600X + 1350Y + 300Z, if N is even.

For CP-1, T = 1350 + 700N + 1600X +1350Y + 300Z, if N is odd.

Execution time for model 730:

For CP-0, T = 700 + 650N + 1500X + 1250Y + 300Z, if N is even.

For CP-0, T = 950 + 650N + 1500X + 1250Y + 300Z, if N is odd.

For CP-1, T = 800 + 700N + 1600X + 1350Y + 300Z, if N is even.

For CP-1, T = 1000 + 700N + 1600X + 1350Y + 300Z, if N is odd.

9. Execution time for model 720:

For CP-0, T = 1050 + 650N, if N is even.

For CP-0, T = 1300 + 650N, if N is odd.

For CP-1, T = 1150 + 700N, if N is even.

For CP-1, T = 1350 + 700N, if N is odd.

Execution time for model 730:

For CP-0, T = 700 + 650N, if N is even.

For CP-0, T = 950 + 650N, if N is odd.

For CP-1, T = 800 + 700N, if N is even.

For CP-1, T = 1000 + 700N, if N is odd.

10. If i equals 1 through 5, the execution time applies to CP-0 and the execution time plus 2 clock periods applies to CP-1.

If i equals 0, the execution times are: model 720, 12 clock periods and model 730, 5 clock periods.

If i equals 6 or 7, the CP-0 execution times are: model 720, 15 clock periods and model 730, 8 clock periods. For CP-1, the same execution times plus 2 clock periods apply.

TABLE 1-3. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 720 AND 730

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
Program Stop and No Operation				
00xxx	Error exit to MA or program stop	-	-	2
460xx	Pass	10	3	-
Increment				
50ijK	Set Ai to (Aj) + K	25	18	10
51ijK	Set Ai to (Bj) + K	25	18	10
52ijK	Set Ai to (Xj) + K	25	18	10
53ijk	Set Ai to (Xj) + (Bk)	25	18	10
54ijk	Set Ai to (Aj) + (Bk)	25	18	10
55ijk	Set Ai to (Aj) - (Bk)	25	18	10
56ijk	Set Ai to (Bj) + (Bk)	25	18	10
57ijk	Set Ai to (Bj) - (Bk)	25	18	10
60ijK	Set Bi to (Aj) + K	11	4	-
61ijK	Set Bi to (Bj) + K	11	4	-
62ijK	Set Bi to (Xj) + K	11	4	-
63ijk	Set Bi to (Xj) + (Bk)	11	4	-
64ijk	Set Bi to (Aj) + (Bk)	11	4	-
65ijk	Set Bi to (Aj) - (Bk)	11	4	-
66ijk	Set Bi to (Bj) + (Bk)	11	4	-
67ijk	Set Bi to (Bj) - (Bk)	11	4	-
70ijK	Set Xi to (Aj) + K	12	5	-
71ijK	Set Xi to (Bj) + K	12	5	-
72ijK	Set Xi to (Xj) + K	12	5	-
73ijk	Set Xi to (Xj) + (Bk)	12	5	-
74ijk	Set Xi to (Aj) + (Bk)	12	5	-

TABLE 1-3. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 720 AND 730 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
75ijk	Set Xi to (Aj) - (Bk)	12	5	-
76ijk	Set Xi to (Bj) + (Bk)	12	5	-
77ijk	Set Xi to (Bj) - (Bk)	12	5	-
Fixed-Point Arithmetic				
36ijk	Integer sum of (Xj) and (Xk) to Xi	12	5	-
37ijk	Integer difference of (Xj) and (Xk) to Xi	12	5	-
47ixk	Population count of (Xk) to Xi	73	67	-
Logical				
10ijx	Transmit (Xj) to Xi	10	3	-
11ijk	Logical product of (Xj) and (Xk) to Xi	12	5	-
12ijk	Logical sum of (Xj) and (Xk) to Xi	12	5	-
13ijk	Logical difference of (Xj) and (Xk) to Xi	12	5	-
14ixk	Transmit complement of (Xk) to Xi	10	3	-
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	12	5	-
16ijk	Logical sum of (Xj) and complement of (Xk) to Xi	12	5	-
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	12	5	-
Shift				
20ijk	Left shift (Xi) by jk	12	5	-
21ijk	Right shift (Xi) by jk	12	5	-

TABLE 1-3. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 720 AND 730 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
22ijk	Left shift (Xk) nominally (Bj) places to Xi	12	5	-
23ijk	Right shift (Xk) nominally (Bj) places to Xi	12	5	-
24ijk	Normalize (Xk) to Xi and Bj	13	6	-
25ijk	Round normalize (Xk) to Xi and Bj	13	6	-
26ijk	Unpack (Xk) to Xi and Bj	12	5	-
27ijk	Pack (Xk) and (Bj) to Xi	12	5	-
43ijk	Form mask of jk bits to Xi	12	5	-
Floating-Point Arithmetic				
30ijk	Floating sum of (Xj) and (Xk) to Xi	16	9	-
31ijk	Floating difference of of (Xj) and (Xk) to Xi	16	9	-
32ijk	Floating double-precision sum of (Xj) and (Xk) to Xi	16	9	-
33ijk	Floating double-precision difference of (Xj) and (Xk) to Xi	16	9	-
34ijk	Round floating sum of (Xj) and (Xk) to Xi	16	9	-
35ijk	Round floating difference of (Xj) and (Xk) to Xi	16	9	-
40ijk	Floating product of (Xj) and (Xk) to Xi	63	57	-

TABLE 1-3. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 720 AND 730 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
41ijk	Round floating product of (Xj) and (Xk) to Xi	63	57	-
42ijk	Floating double-precision product of (Xj) and (Xk) to Xi	63	57	-
44ijk	Floating divide (Xj) by (Xk) to Xi	63	57	-
45ijk	Round floating divide (Xj) by (Xk) to Xi	63	57	-
Branch/Jump				
010xK	Return jump to K	32 (CP-0) 36 (CP-1)	25 (CP-0) 29 (CP-1)	-
013jK	Central exchange jump to (Bj) + K (monitor flag set)	45	45	-
013xx	Central exchange jump to MA (monitor flag not set)	45	45	-
02ixK	Jump to (Bi) + K	27 (CP-0) 29 (CP-1)	22	4
030jK	Branch to K if (Xj) = 0	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
031jK	Branch to K if (Xj) ≠ 0	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
032jK	Branch to K if (Xj) positive	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
033jK	Branch to K if (Xj) negative	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
034jK	Branch to K if (Xj) in range	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
035jK	Branch to K if (Xj) out of range	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
036jK	Branch to K if (Xj) definite	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4

TABLE 1-3. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 720 AND 730 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)		Notes
		720	730	
037jK	Branch to K if (Xj) indefinite	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
04ijK	Branch to K if (Bi) = (Bj)	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
05ijK	Branch to K if (Bi) $\neq$ (Bj)	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
06ijK	Branch to K if (Bi) $\geqq$ (Bj)	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
07ijK	Branch to K if (Bi) < (Bj)	27 (CP-0) 29 (CP-1)	20 (CP-0) 22 (CP-1)	4
ECS Communication				
011jK	Block copy (Bj) + K words from ECS to CM	2[(BJ)+K]	2[(BJ)+K]	3
012jK	Block copy (Bj) + K words from CM to ECS	2[(BJ)+K]	2[(BJ)+K]	3
Compare/Move				
464jK	Move indirect	-	-	5,6
465	Move direct	-	-	5,7
466	Compare collated	-	-	5,8
467	Compare uncollated	-	-	5,9

Notes:

Refer to applicable notes at end of table 1-2.

TABLE 1-4. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 740, 750, AND 760

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
00xxx	Error exit to MA or program stop	-		-	-
010xK	Return jump to K	28	28	20	1,2,3
011jK	Block copy (Bj) + K words from ECS to CM	4[(Bj)+K]	4[(Bj)+K]	4[(Bj)+K]	4,5,6,7,9
012jK	Block copy (Bj) + K words from CM to ECS	4[(Bj)+K]	4[(Bj)+K]	4[(Bj)+K]	4,5,6,7,9
013jK	Central exchange jump to (Bj) + K (monitor flag set)	91	91	83	1,2,4
013xx	Central exchange jump to MA (monitor flag not set)	91	91	83	1,2,4
02ixK	Jump to (Bi) + K	26	26	18	1,2,3,8, 18
030jK	Branch to K if (Xj) = 0	26	26	18	1,2,3,10, 11,18
031jK	Branch to K if (Xj) = 0	26	26	18	1,2,3,10, 11,18
032jK	Branch to K if (Xj) positive	26	26	18	1,2,3,10, 11,18
033jK	Branch to K if (Xj) negative	26	26	18	1,2,3,10, 11,18
034jK	Branch to K if (Xj) in range	26	26	18	1,2,3,10, 11,18
035jK	Branch to K if (Xj) out of range	26	26	18	1,2,3,10, 11,18
036jK	Branch to K if (Xj) definite	26	26	18	1,2,3,10, 11,18
037jK	Branch to K if (Xj) indefinite	26	26	18	1,2,3,10, 11,18
04ijK	Branch to K if (Bi) = (Bj)	26	26	18	1,2,3,10, 11,18

TABLE 1-4. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 740, 750, AND 760 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
05ijK	Branch to K if (Bi) ≠ (Bj)	26	26	18	1,2,3,10, 11,18
06ijK	Branch to K if (Bi) ≧ (Bj)	26	26	18	1,2,3,10, 11,18
07ijK	Branch to K if (Bi) < (Bj)	26	26	18	1,2,3,10, 11,18
10ijx	Transmit (Xj) to Xi	10	2	2	8,12,13, 19,22,23
11ijk	Logical product of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23
12ijk	Logical sum of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23
13ijk	Logical difference of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23
14ixk	Transmit complement of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
16ijk	Logical sum of (Xj) and complement of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
20ijk	Left shift (Xi) by jk	10	2	2	8,12,13, 19,22,23
21ijk	Right shift (Xi) by jk	10	2	2	8,12,13, 19,22,23
22ijk	Left shift (Xk) nominally (Bj) places to Xi	10	2	2	8,12,13, 19,22,23
23ijk	Right shift (Xk) nominally (Bj) places to Xi	10	2	2	8,12,13, 22,23

TABLE 1-4. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 740, 750, AND 760 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
24ijk	Normalize (Xk) to Xi and Bj	10	3	3	8,12,13, 20,22,23
25ijk	Round normalize (Xk) to Xi and Bj	10	3	3	8,12,13, 20,22,23
26ijk	Unpack (Xk) to Xi and Bj	10	2	2	8,12,13, 19,22,23
27ijk	Pack (Xk) and (Bj) to Xi	10	2	2	8,12,13, 19,22,23
30ijk	Floating sum of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
31ijk	Floating difference of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
32ijk	Floating double-precision sum of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
33ijk	Floating double-precision difference of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
34ijk	Round floating sum of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
35ijk	Round floating difference of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
36ijk	Integer sum of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23
37ijk	Integer difference of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23
40ijk	Floating product of (Xj) and (Xk) to Xi	12	5	5	8,12,13, 14,22,23
41ijk	Round floating product of (Xj) (Xk) to Xi	12	5	5	8,12,13, 14,22,23
42ijk	Floating double-precision product of (Xj) and (Xk) to Xi	12	5	5	8,12,13, 14,22,23

TABLE 1-4. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 740, 750, AND 760 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
43ijk	Form mask of jk bits to Xi	10	2	2	8,12,13, 19,22,23
44ijk	Floating divide (Xj) by (Xk) to Xi	28	20	20	8,12,13, 15
45ijk	Round floating divide (Xj) by (Xk) to Xi	28	20	20	8,12,13, 15
460xx	Pass	10	1	-	-
47ixk	Population count of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
50ijK	Set Ai to (Aj) + K	23	23	15	2,3,8,16, 17,18,23
51ijK	Set Ai to (Bj) + K	23	23	15	2,3,8,16, 17,18,23
52ijK	Set Ai to (Xj) + K	23	23	15	2,3,8,16, 17,18,23
53ijk	Set Ai to (Xj) + (Bk)	23	23	15	2,3,8,16, 17,18,23
54ijk	Set Ai to (Aj) + (Bk)	23	23	15	2,3,8,16, 17,18,23
55ijk	Set Ai to (Aj) - (Bk)	23	23	15	2,3,8,16, 17,18,23
56ijk	Set Ai to (Bj) + (Bk)	23	23	15	2,3,8,16, 17,18,23
57ijk	Set Ai to (Bj) - (Bk)	23	23	15	2,3,8,16, 17,18,23
60ijK	Set Bi to (Aj) + K	10	2	2	8,12,13, 19,22,23
61ijK	Set Bi to (Bj) + K	10	2	2	8,12,13, 19,22,23
62ijK	Set Bi to (Xj) + K	10	2	2	8,12,13, 19,22,23
63ijk	Set Bi to (Xj) + (Bk)	10	2	2	8,12,13, 19,22,23

TABLE 1-4. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 740, 750, AND 760 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
64ijk	Set Bi to (Aj) + (Bk)	10	2	2	8,12,13, 19,22,23
65ijk	Set Bi to (Aj) - (Bk)	10	2	2	8,12,13, 19,22,23
66ijk	Set Bi to (Bj) + (Bk)	10	2	2	8,12,13, 19,22,23
67ijk	Set Bi to (Bj) - (Bk)	10	2	2	8,12,13, 19,22,23
70ijK	Set Xi to (Aj) + K	10	2	2	8,12,13, 19,22,23
71ijK	Set Xi to (Bj) + K	10	2	2	8,12,13, 19,22,23
72ijK	Set Xi to (Xj) + K	10	2	2	8,12,13, 19,22,23
73ijk	Set Xi to (Xj) + (Bk)	10	2	2	8,12,13, 19,22,23
74ijk	Set Xi to (Aj) + (Bk)	10	2	2	8,12,13, 19,22,23
75ijk	Set Xi to (Aj) - (Bk)	10	2	2	8,12,13, 19,22,23
76ijk	Set Xi to (Bj) + (Bk)	10	2	2	8,12,13, 19,22,23
77ijk	Set Xi to (Bj) - (Bk)	10	2	2	8,12,13, 19,22,23

Notes:

1. All previous instruction fetches are complete.
2. No CM conflicts or storage address stack (SAS) backup caused by CM conflicts exist.
3. No PPS request occurs.
4. All operating registers are free.
5. ECS is not busy.

TABLE 1-4. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 740, 750, AND 760 (Contd)

6. All ECS banks have completed previously initiated read/write cycles.

7. The time does not include start-up time.

8. The requested operating register(s) is free.

9. The time assumes no ECS record gaps.

10. If the address is in the IAS, the execution time is 3 clock periods.

11. If the branch conditions are not met, the execution time is 2 clock periods for model 750/760 and 10 clock periods for model 740.

12. The requested destination register(s) input data path is free during the required clock period.

13. After the instruction is issued to the functional unit, no further delay is possible.

14. The multiply unit is free.

15. The divide unit is free.

16. This execution time applies only when i equals 1 through 5. A storage reference is required.

    If i equals 0, the execution time is 2 clock periods for model 750/760 and 10 clock periods for model 740. No storage reference is required.

    If i equals 6 or 7, the execution time is 2 clock periods for model 750/760 and 10 clock periods for model 740. A storage reference continues after instruction execution.

17. After the instruction is issued to the increment unit, no further delays are possible in the delivery of data to the Ai register. However, CM conflicts may delay the resulting storage reference.

18. If memory enable is present when the address is gated into SAS, one additional 25-nanosecond clock period is required. This condition occurs about 50 percent of the time.

19. This applies to model 740 only. If the instruction follows a normalize instruction, add 2 clock periods to the execution time.

20. This applies to model 740 only. If the instruction follows a floating add instruction, add 2 clock periods to the execution time.

TABLE 1-4. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 740, 750, AND 760 (Contd)

21.	This applies to model 740 only. If the instruction follows a multiply instruction, add 2 clock periods to the execution time.
22.	This applies to model 740 only. If the instruction (other than a divide or one which does a memory reference) follows one which performed a memory read reference, subtract 1 clock period.
23.	This applies to model 740 only. If this instruction follows a divide instruction, add 1 clock period to the execution time listed for model 750.

TABLE 1-5. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 740, 750, AND 760

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
Program Stop and No Operation					
00xxx	Error exit to MA or program stop	-		-	-
460xx	Pass	10	1	-	-
Increment					
50ijK	Set Ai to (Aj) + K	23	23	15	2,3,8,16, 17,18,23
51ijK	Set Ai to (Bj) + K	23	23	15	2,3,8,16, 17,18,23
52ijK	Set Ai to (Xj) + K	23	23	15	2,3,8,16, 17,18,23
53ijk	Set Ai to (Xj) + (Bk)	23	23	15	2,3,8,16, 17,18,23
54ijk	Set Ai to (Aj) + (Bk)	23	23	15	2,3,8,16, 17,18,23
55ijk	Set Ai to (Aj) - (Bk)	23	23	15	2,3,8,16, 17,18,23
56ijk	Set Ai to (Bj) + (Bk)	23	23	15	2,3,8,16, 17,18,23
57ijk	Set Ai to (Bj) - (Bk)	23	23	15	2,3,8,16, 17,18,23
60ijK	Set Bi to (Aj) + K	10	2	2	8,12,13, 19,22,23
61ijK	Set Bi to (Bj) + K	10	2	2	8,12,13, 19,22,23
62ijK	Set Bi to (Xj) + K	10	2	2	8,12,13, 19,22,23
63ijk	Set Bi to (Xj) + (Bk)	10	2	2	8,12,13, 19,22,23
64ijk	Set Bi to (Aj) + (Bk)	10	2	2	8,12,13, 19,22,23
65ijk	Set Bi to (Aj) - (Bk)	10	2	2	8,12,13, 19,22,23

TABLE 1-5. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 740, 750, AND 760 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
66ijk	Set Bi to (Bj) + (Bk)	10	2	2	8,12,13, 19,22,23
67ijk	Set Bi to (Bj) - (Bk)	10	2	2	8,12,13, 19,22,23
70ijK	Set Xi to (Aj) + K	10	2	2	8,12,13, 19,22,23
71ijK	Set Xi to (Bj) + K	10	2	2	8,12,13, 19,22,23
72ijK	Set Xi to (Xj) + K	10	2	2	8,12,13, 19,22,23
73ijk	Set Xi to (Xj) + (Bk)	10	2	2	8,12,13, 19,22,23
74ijk	Set Xi to (Aj) + (Bk)	10	2	2	8,12,13, 19,22,23
75ijk	Set Xi to (Aj) - (Bk)	10	2	2	8,12,13, 19,22,23
76ijk	Set Xi to (Bj) + (Bk)	10	2	2	8,12,13, 19,22,23
77ijk	Set Xi to (Bj) - (Bk)	10	2	2	8,12,13, 19,22,23
Fixed-Point Arithmetic					
36ijk	Integer sum of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23
37ijk	Integer difference of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23
47ixk	Population count of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
Logical					
10ijx	Transmit (Xj) to Xi	10	2	2	8,12,13, 19,22,23
11ijk	Logical product of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23

TABLE 1-5. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 740, 750, AND 760 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
12ijk	Logical sum of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23
13ijk	Logical difference of (Xj) and (Xk) to Xi	10	2	2	8,12,13, 19,22,23
14ixk	Transmit complement of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
16ijk	Logical sum of (Xj) and complement of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	10	2	2	8,12,13, 19,22,23
Shift					
20ijk	Left shift (Xi) by jk	10	2	2	8,12,13, 19,22,23
21ijk	Right shift (Xi) by jk	10	2	2	8,12,13, 19,22,23
22ijk	Left shift (Xk) nominally (Bj) places to Xi	10	2	2	8,12,13, 19,22,23
23ijk	Right shift (Xk) nominally (Bj) places to Xi	10	2	2	8,12,13, 19,22,23
24ijk	Normalize (Xk) to Xi and Bj	10	3	3	8,12,13, 20,22,23
25ijk	Round normalize (Xk) to Xi and Bj	10	3	3	8,12,13, 20,22,23
26ijk	Unpack (Xk) to Xi and Bj	10	2	2	8,12,13, 20,22,23
27ijk	Pack (Xk) and (Bj) to Xi	10	2	2	8,12,13, 20,22,23
43ijk	Form mask of jk bits to Xi	10	2	2	8,12,13, 19,22,23

TABLE 1-5. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 740, 750, AND 760 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
Floating-Point Arithmetic					
30ijk	Floating sum of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
31ijk	Floating difference of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
32ijk	Floating double-precision sum of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
33ijk	Floating double-precision difference of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
34ijk	Round floating sum of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
35ijk	Round floating difference of (Xj) and (Xk) to Xi	10	4	4	8,12,13, 21,22,23
40ijk	Floating product of (Xj) and (Xk) to Xi	12	5	5	8,12,13, 14,22,23
41ijk	Round floating product of (Xj) and (Xk) to Xi	12	5	5	8,12,13, 14,22,23
42ijk	Floating double-precision product of (Xj) and (Xk) to Xi	12	5	5	8,12,13, 14,22,23
44ijk	Floating divide (Xj) by (Xk) to Xi	28	20	20	8,12,13, 15
45ijk	Round floating divide (Xj) by (Xk) to Xi	28	20	20	8,12,13, 15
Branch/Jump					
010xK	Return jump to K	28	28	20	1,2,3
013jK	Central exchange jump to (Bj) + K (monitor flag set)	91	91	83	1,2,4
013xx	Central exchange jump to MA (monitor flag not set)	91	91	83	1,2,4

TABLE 1-5. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 740, 750, AND 760 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)			Notes
		740	750	760	
02ixK	Jump to (Bi) + K	26	26	18	1,2,3,8,18
030jK	Branch to K if (Xj) = 0	26	26	18	1,2,3,10,11,18
031jK	Branch to K if (Xj) ≠ 0	26	26	18	1,2,3,10,11,18
032jK	Branch to K if (Xj) positive	26	26	18	1,2,3,10,11,18
033jK	Branch to K if (Xj) negative	26	26	18	1,2,3,10,11,18
034jK	Branch to K if (Xj) in range	26	26	18	1,2,3,10,11,18
035jK	Branch to K if (Xj) out of range	26	26	18	1,2,3,10,11,18
036jK	Branch to K if (Xj) definite	26	26	18	1,2,3,10,11,18
037jK	Branch to K if (Xj) indefinite	26	26	18	1,2,3,10,11,18
04ijK	Branch to K if (Bi) = (Bj)	26	26	18	1,2,3,10,11,18
05ijK	Branch to K if (Bi) ≠ (Bj)	26	26	18	1,2,3,10,11,18
06ijK	Branch to K if (Bi) ≧ (Bj)	26	26	18	1,2,3,10,11,18
07ijK	Branch to K if (Bi) < (Bj)	26	26	18	1,2,3,10,11,18
ECS Communication					
011jK	Block copy (Bj) + K words from ECS to CM	4[(Bj)+K]	4[(Bj)+K]	4[(Bj)+K]	4,5,6,7,9
012jK	Block copy (Bj) + K words from CM to ECS	4[(Bj)+K]	4[(Bj)+K]	4[(Bj)+K]	4,5,6,7,9

Notes:

Refer to applicable notes at end of table 1-4.

TABLE 1-6. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 LEVEL B/C

Instruction Code	Description	Execution Time (Clock Periods)	Notes
00xxx	Error exit to EEA	-	-
010xK	Return jump to K	13	1,2,3
011jK	Block copy (Bj) + K words from LCME to CM	(Bj)+K+22	1,2,3,4,5, 6,19,22
012jK	Block copy (Bj) + K words from CM to LCME	(Bj)+K+13	1,2,3,4,5, 6,19,22
013jK	Exchange exit to (Bj) + K (exit mode flag set)	28	1,2,3,4
013xx	Exchange exit to NEA (exit mode flag not set)	28	1,2,3,4
014jk	Read LCME at (Xk) to Xj	23	5,7,8,9
015jk	Write Xj into LCME at (Xk)	3	5,7,8,21
0160k	Reset input channel (Bk) buffer	4	8
016jk	Read input channel (Bk) status to Bj ($j \neq 0$)	3	8
0170k	Reset output channel (Bk) buffer	16	8
017jk	Read output channel (Bk) status to Bj ($j \neq 0$)	3	8
02ixK	Jump to (Bk) + K	11	1,2,8,10
030jK	Branch to K if (Xj) = 0	11	1,2,10,11
031jK	Branch to K if (Xj) $\neq$ 0	11	1,2,10,11
032jK	Branch to K if (Xj) positive	11	1,2,10,11

TABLE 1-6. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 LEVEL B/C (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
033jK	Branch to K if (Xj) negative	11	1,2,10,11
034jK	Branch to K if (Xj) in range	11	1,2,10,11
035jK	Branch to K if (Xj) out of range	11	1,2,10,11
036jK	Branch to K if (Xj) definite	11	1,2,10,11
037jK	Branch to K if (Xj) indefinite	11	1,2,10,11
04ijK	Branch to K if (Bi) = (Bj)	11	1,2,10,11
05ijK	Branch to K if (Bi) ≠ (Bj)	11	1,2,10,11
06ijK	Branch to K if (Bi) = (Bj)	11	1,2,10,11
07ijK	Branch to K if (Bi) (Bj)	11	1,2,10,11
10ijx	Transmit (Xj) to Xi	2	2,8,12,13
11ijk	Logical product of (Xj) and (Xk) to Xi	2	2,8,12,13
12ijk	Logical sum of (Xj) and (Xk) to Xi	2	2,8,12,13
13ijk	Logical difference of (Xj) and (Xk) to Xi	2	2,8,12,13
14ijk	Transmit complement of (Xk) to Xi	2	2,8,12,13
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	2	2,8,12,13
16ijk	Logical sum of (Xj) and complement of (Xj) to Xi	2	2,8,12,13

TABLE 1-6. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 LEVEL B/C (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	2	2,8,12,13
20ijk	Left shift (Xi) by jk	2	2,8,12,13
21ijk	Right shift (Xi) by jk	2	2,8,12,13
22ijk	Left shift (Xk) nominally (Bj) places to Xi	2	2,8,12,13
23ijk	Right shift (Xk) nominally (Bj) places to Xi	2	2,8,12,13
24ijk	Normalize (Xk) to Xi and Bj	3	2,8,12,13
25ijk	Round normalize (Xk) to Xi and Bj	3	2,8,12,13
26ijk	Unpack (Xk) to Xi and Bj	2	2,8,12,13
27ijk	Pack (Xk) and (Bj) to Xi	2	2,8,12,13
30ijk	Floating sum of (Xj) and (Xk) to Xi	4	2,8,12,13
31ijk	Floating difference of (Xj) and (Xk) to Xi	4	2,8,12,13
32ijk	Floating double-precision sum of (Xj) and (Xk) to Xi	5	2,8,12,13
33ijk	Floating double-precision difference of (Xi) and (Xk) to Xi	5	2,8,12,13
34ijk	Round floating sum of (Xj) and (Xk) to Xi	5	2,8,12,13
35ijk	Round floating difference of (Xj) and (Xk) to Xi	5	2,8,12,13

TABLE 1-6. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 LEVEL B/C (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
36ijk	Integer sum of (Xj) and (Xk) to Xi	2	2,8,12,13
37ijk	Integer difference of (Xj) and (Xk) to Xi	2	2,8,12,13
40ijk	Floating product of (Xj) and (Xk) to Xi	5	2,8,12,13, 14
41ijk	Round floating product of (Xj) and (Xk) to Xi	5	2,8,12,13, 14
42ijk	Floating double-precision product of (Xj) and (Xk) to Xi	5	2,8,12,13, 14
43ijk	Form mask of jk bits to Xi	2	2,8,12,13
44ijk	Floating divide (Xj) by (Xk) to Xi	20	2,8,12,13, 15
45ijk	Round floating divide (Xj) by (Xk) to Xi	20	2,8,12,13, 15
46xxx	Pass	1	-
47ixk	Population count of (Xk) to Xi	2	2,8,12,13
50ijK	Set Ai to (Aj) + K	8	2,8,16,17, 18
51ijK	Set Ai to (Bj) + K	8	2,8,16,17, 18
52ijK	Set Ai to (Xj) + K	8	2,8,16,17, 18
53ijk	Set Ai to (Xj) + (Bk)	8	2,8,16,17, 18
54ijk	Set Ai to (Aj) + (Bk)	8	2,8,16,17, 18
55ijk	Set Ai to (Aj) - (Bk)	8	2,8,16,17, 18
56ijk	Set Ai to (Bj) + (Bk)	8	2,8,16,17, 18

TABLE 1-6. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 LEVEL B/C (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
57ijk	Set Ai to (Bj) - (Bk)	8	2,8,16,17, 18
60ijK	Set Bi to (Aj) + K	2	2,8,12,13
61ijK	Set Bi to (Bj) + K	2	2,8,12,13
62ijK	Set Bi to (Xj) + K	2	2,8,12,13
63ijk	Set Bi to (Xj) + (Bk)	2	2,8,12,13
64ijk	Set Bi to (Aj) + (Bk)	2	2,8,12,13
65ijk	Set Bi to (Aj) - (Bk)	2	2,8,12,13
66ijk	Set Bi to (Bj) + (Bk)	2	2,8,12,13
67ijk	Set Bi to (Bj) - (Bk)	2	2,8,12,13
70ijK	Set Xi to (Aj) + K	2	2,8,12,13
71ijK	Set Xi to (Bj) + K	2	2,8,12,13
72ijK	Set Xi to (Xj) + K	2	2,8,12,13
73ijk	Set Xi to (Xj) + (Bk)	2	2,8,12,13
74ijk	Set Xi to (Aj) + (Bk)	2	2,8,12,13
75ijk	Set Xi to (Aj) - (Bk)	2	2,8,12,13
76ijk	Set Xi to (Bj) + (Bk)	2	2,8,12,13
77ijk	Set Xi to (Bj) - (Bk)	2	2,8,12,13

Notes:

1. All previous instruction fetches are complete.
2. No CM conflicts or SAS backup caused by CM conflicts exist.
3. No I/O word request occurs.
4. All operating registers are free.
5. LCME is not busy.
6. All LCME banks have completed previously initiated read/write cycles.

TABLE 1-6. CP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 LEVEL B/C (Contd)

7. The requested LCME bank has completed a previously initiated read/write cycle.

8. The requested operating register(s) is free.

9. If the requested word is in an LCME bank operand register because of a previous reference, the execution time is 6 clock periods and could be as many as 15 clock periods if the bank is busy with a previous instruction, provided no other conflicts occur.

10. If the address is in the IAS, the execution time is 3 clock periods.

11. If the branch conditions are not met, the execution time is 2 clock periods.

12. The requested destination register(s) input data path is free during the required clock period.

13. After the instruction is issued to the functional unit, no further delay is possible.

14. The multiply unit is free.

15. The divide unit is free.

16. If no storage reference is required (i is 0), the execution time is 2 clock periods.

17. After the instruction is issued to the increment unit, no further delays are possible in the delivery of data to the Ai register. However, CM conflicts may delay the resulting storage reference.

18. Execution time 8 refers to read instructions only. With respect to the CPU, a write instruction is completed when Ai sets (2 clock periods). A CM read requires 6 clock periods, and a CM write requires 9 clock periods to complete a bank reference after the increment instruction is in the CIW register.

19. If the word count is greater than 45 minus W (W equals the starting word), the execution time is (Bj) plus K plus 26 clock periods.

20. If the transfer does not end with word 17_8, add 17_8 minus W clock periods (W equals the last word transferred).

21. If the requested bank is busy with a previous instruction, the execution time could be as many as 37 additional clock periods.

22. Models with 512K of LCME have a maximum transfer rate of approximately 32 words per 64 clock periods.

TABLE 1-7. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODEL 176 LEVEL B/C

Instruction Code	Description	Execution Time (Clock Periods)	Notes
Program Stop and No Operation			
00xxx	Error exit to MA or program stop	-	-
46xxx	Pass	1	-
Increment			
50ijK	Set Ai to (Aj) + K	8	2,8,16,17, 18
51ijK	Set Ai to (Bj) + K	8	2,8,16,17, 18
52ijK	Set Ai to (Xj) + K	8	2,8,16,17, 18
53ijk	Set Ai to (Xj) + (Bk)	8	2,8,16,17, 18
54ijk	Set Ai to (Aj) + (Bk)	8	2,8,16,17, 18
55ijk	Set Ai to (Aj) - (Bk)	8	2,8,16,17, 18
56ijk	Set Ai to (Bj) + (Bk)	8	2,8,16,17, 18
57ijk	Set Ai to (Bj) - (Bk)	8	2,8,16,17, 18
60ijK	Set Bi to (Aj) + K	2	2,8,12,13
61ijK	Set Bi to (Bj) + K	2	2,8,12,13
62ijK	Set Bi to (Xj) + K	2	2,8,12,13
63ijk	Set Bi to (Xj) + (Bk)	2	2,8,12,13
64ijk	Set Bi to (Aj) + (Bk)	2	2,8,12,13
65ijk	Set Bi to (Aj) - (Bk)	2	2,8,12,13
66ijk	Set Bi to (Bj) + (Bk)	2	2,8,12,13
67ijk	Set Bi to (Bj) - (Bk)	2	2,8,12,13
70ijK	Set Xi to (Aj) + K	2	2,8,12,13
71ijK	Set Xi to (Bj) + K	2	2,8,12,13

TABLE 1-7. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODEL 176 LEVEL B/C (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
72ijK	Set Xi to (Xj) + K	2	2,8,12,13
73ijk	Set Xi to (Xj) + (Bk)	2	2,8,12,13
74ijk	Set Xi to (Aj) + (Bk)	2	2,8,12,13
75ijk	Set Xi to (Aj) - (Bk)	2	2,8,12,13
76ijk	Set Xi to (Bj) + (Bk)	2	2,8,12,13
77ijk	Set Xi to (Bj) - (Bk)	2	2,8,12,13
Fixed-Point Arithmetic			
36ijk	Integer sum of (Xj) and (Xk) to Xi	2	2,8,12,13
37ijk	Integer difference of (Xj) and (Xk) to Xi	2	2,8,12,13
47ixk	Population count of (Xk) to Xi	2	2,8,12,13
Logical			
10ijx	Transmit (Xj) to Xi	2	2,8,12,13
11ijk	Logical product of (Xj) and (Xk) to Xi	2	2,8,12,13
12ijk	Logical sum of (Xj) and (Xk) to Xi	2	2,8,12,13
13ijk	Logical difference of (Xj) and (Xk) to Xi	2	2,8,12,13
14ixk	Transmit complement of (Xk) to Xi	2	2,8,12,13
15ijk	Logical product of (Xj) and complement of (Xk) to Xi	2	2,8,12,13
16ijk	Logical sum of (Xj) and complement of (Xk) to Xi	2	2,8,12,13
17ijk	Logical difference of (Xj) and complement of (Xk) to Xi	2	2,8,12,13

TABLE 1-7. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODEL 176 LEVEL B/C (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
Shift			
20ijk	Left shift (Xi) by jk	2	2,8,12,13
21ijk	Right shift (Xi) by jk	2	2,8,12,13
22ijk	Left shift (Xk) nominally (Bj) places to Xi	2	2,8,12,13
23ijk	Right shift (Xk) nominally (Bj) places to Xi	2	2,8,12,13
24ijk	Normalize (Xk) to Xi and Bj	3	2,8,12,13
25ijk	Round normalize (Xk) to Xi and Bj	3	2,8,12,13
26ijk	Unpack (Xk) to Xi and Bj	2	2,8,12,13
27ijk	Pack (Xk) and (Bj) to Xi	2	2,8,12,13
43ijk	Form mask of jk bits to Xi	2	2,8,12,13
Floating-Point Arithmetic			
30ijk	Floating sum of (Xj) and (Xk) to Xi	4	2,8,12,13
31ijk	Floating difference of of (Xj) and (Xk) to Xi	4	2,8,12,13
32ijk	Floating double-precision sum of (Xj) and (Xk) to Xi	5	2,8,12,13
33ijk	Floating double-precision difference of (Xj) and (Xk) to Xi	5	2,8,12,13
34ijk	Round floating sum of (Xj) and (Xk) to Xi	5	2,8,12,13
35ijk	Round floating difference of (Xj) and (Xk) to Xi	5	2,8,12,13

TABLE 1-7. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODEL 176 LEVEL B/C (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
40ijk	Floating product of (Xj) and (Xk) to Xi	5	2,8,12,13, 14
41ijk	Round floating product of (Xj) and (Xk) to Xi	5	2,8,12,13, 14
42ijk	Floating double-precision product of (Xj) and (Xk) to Xi	5	2,8,12,13, 14
44ijk	Floating divide (Xj) by (Xk) to Xi	20	2,8,12,13, 15
45ijk	Round floating divide (Xj) by (Xk) to Xi	20	2,8,12,13, 15
Branch/Jump			
010xK	Return jump to K	13	1,2,3
013jK	Central exchange jump to (Bj) + K (monitor flag set)	28	1,2,3,4
013xx	Central exchange jump to MA (monitor flag not set)	28	1,2,3,4
02ixK	Jump to (Bi) + K	11	1,2,8,10
030jK	Branch to K if (Xj) = 0	11	1,2,10,11
031jK	Branch to K if (Xj) $\neq$ 0	11	1,2,10,11
032jK	Branch to K if (Xj) positive	11	1,2,10,11
033jK	Branch to K if (Xj) negative	11	1,2,10,11
034jK	Branch to K if (Xj) in range	11	1,2,10,11
035jK	Branch to K if (Xj) out of range	11	1,2,10,11
036jK	Branch to K if (Xj) definite	11	1,2,10,11

TABLE 1-7. CP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODEL 176 LEVEL B/C (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
037jK	Branch to K if (Xj) indefinite	11	1,2,10,11
04ijK	Branch to K if (Bi) = (Bj)	11	1,2,10,11
05ijK	Branch to K if (Bi) ≠ (Bj)	11	1,2,10,11
06ijK	Branch to K if (Bi) ≧ (Bj)	11	1,2,10,11
07ijK	Branch to K if (Bi) < (Bj)	11	1,2,10,11
LCME Communication			
011jK	Block copy (Bj) + K words from LCME to CM	(Bj)+K+22	1,2,3,4,5, 6,19,22
012jK	Block copy (Bj) + K words from CM to LCME	(Bj)+K+22	1,2,3,4,5, 6,19,22
014jk	Read LCME at (Xk) to Xj	23	5,7,8,9
015jk	Write Xj into LCME at (Xk)	3	5,7,8,21
I/O Channel Buffer			
0160k	Reset input channel (Bk) buffer	4	8
016jk	Read input channel (Bk) status to Bj (j ≠ 0)	3	8
0170k	Reset output channel (Bk) buffer	16	8
017jk	Read output channel (Bk) status to Bj (j ≠ 0)	3	8

Notes:

Refer to applicable notes at end of table 1-6.

PERIPHERAL PROCESSOR UNIT AND PERIPHERAL PROCESSOR INSTRUCTIONS 2

This segment of the manual describes both the peripheral processor unit (PPU) and peripheral processor (PP) instructions. The PPU instructions apply to model 176. The PP instructions apply to the peripheral processor subsystems (PPS) of models 720 through 760. These instruction sets are the same and produce the same results, except for the instructions listed in table 2-1.

TABLE 2-1. PPU AND PP INSTRUCTION DIFFERENCES

Instruction Code	PPU Instruction Description	PP Instruction Description
00	00xx Error stop	0000 Pass
24	24xx Pass	2400 Pass
25	25xx Pass	2500 Pass
26	26xx Pass	260x Exchange jump
		261x Monitor exchange jump
		262x Monitor exchange jump to MA
27	27xx Pass	27x Read program address
60	60dm Jump to m if channel d input word flag set	60d Central read from (A) to d
61	61dm Jump to m if channel d input word flag not set	61dm Central read (d) words from (A) to m
62	62dm Jump to m if channel d input record flag set	62d Central write to (A) from d
63	63dm Jump to m if channel d input record flag not set	63dm Central write (d) words to (A) from m
64	64dm Jump to m if channel d output word flag set	64dm Jump to m if channel d active
65	65dm Jump to m if channel d output word flag not set	65dm Jump to m if channel d inactive
66	66dm Jump to m if channel d output record flag set	66dm Jump to m if channel d full
67	67dm Jump to m if channel d output record flag not set	67dm Jump to m if channel d empty

TABLE 2-1. PPU AND PP INSTRUCTION DIFFERENCES
(Contd)

Instruction Code	PPU Instruction Description	PP Instruction Description
74	74d Set output record flag on channel d	74d Activate channel d
75	75xx Pass	75d Disconnect channel d
76	76xx Pass	76d Function (A) on channel d
77	77xx Error stop	77dm Function m on channel d

INSTRUCTION FORMATS

The PPU and PP instructions use 12- and 24-bit formats. The 12-bit format (figure 2-1) has a 6-bit operation code f and a 6-bit operand or operand address d. The 24-bit format (figure 2-2) uses the 12-bit quantity m, the content of the next program address (P plus 1), with d to form an 18-bit operand address.

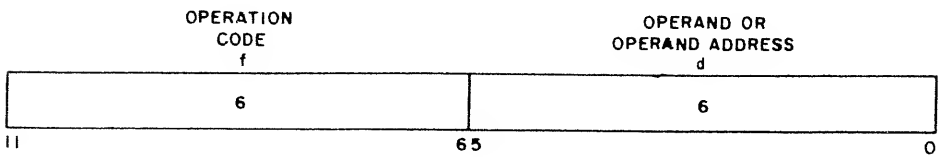

Figure 2-1. PPU and PP 12-Bit Instruction Format

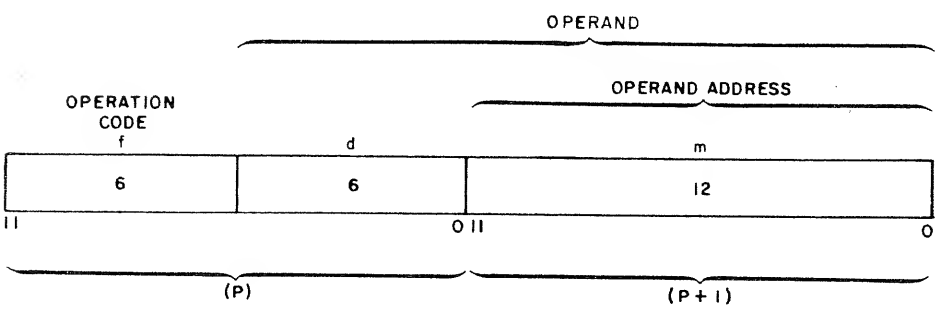

Figure 2-2. PPU and PP 24-Bit Instruction Format

INSTRUCTION DESIGNATOR DESCRIPTIONS

Table 2-2 lists the instruction designators used in the PPU and PP instruction sets.

TABLE 2-2. PPU AND PP INSTRUCTION DESIGNATORS

Designator	Use
f	6-bit operation code.
d	6-bit operand or address.
m	12-bit operand or address.
fd	12-bit instruction code.
dm	18-bit operand.
x	Unused register.
A	Arithmetic register.
P	Program register.
Q	Q register.
( )	Content of a register or location.
(( ))	Indirect addressing which specifies the content of a location whose address is specified by a designator inside the parentheses.

Designator usage:

d	Implies d itself.
(d)	Implies the content of d.
((d))	Implies the contents of the location specified by d.
m	Implies m itself used as an address.
m + (d)	The contents of d are added to m to form an operand (jump address).

(m + (d))	The contents of d are added to m to form the address of the operand.
dm	Implies an 18-bit quantity with d as the upper 6 bits and m as the lower 12 bits.

PPU INSTRUCTIONS AND EXECUTION TIMES

The PP instructions and their execution times are listed in numeric sequence in table 2-3. The notes refer to the notes at the end of the table. Execution times are in 27.5-nanosecond clock periods.

The execution timing for the PPU instructions is dominated by the access time of the semiconductor storage banks. There are two independent banks of storage. One bank contains all even storage addresses, and the other bank contains all odd storage addresses. If references to storage alternate between even and odd addresses, each reference requires 5 clock periods. If two even references (or two odd references) occur consecutively, the storage read/write cycle for the first reference must be completed before the second reference can begin. In this case, a storage reference requires 10 clock periods. As a result, the execution time for most of the PPU instructions is a multiple of clock periods with variation in increments of 5 clock periods, depending upon the storage addresses involved.

Table 2-4 contains the same information, except that it groups the instructions by their functions.

TABLE 2-3. PPU INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176

Instruction Code	Description	Execution Time (Clock Periods)	Notes
00xx	Error stop	-	-
0100m	Long jump to m	10 or 15	1,2
01dm	Long jump to m + (d)	15, 20, or 25	1,2
0200m	Return jump to m	15 or 20	1,2
02dm	Return jump to m + (d)	20, 25, or 30	1,2
03d	Unconditional jump d	7 or 10	2
04d	Zero jump d	5	3,4
05d	Nonzero jump d	5	3
06d	Plus jump d	5	3
07d	Minus jump d	5	3
10d	Shift (A) by d	6	5
11d	Logical difference (A) and d	5	6
12d	Logical product (A) and d	5	6
13d	Selective clear (A) by d	5	6
14d	Load d	5	6
15d	Load complement d	5	6
16d	Add (A) + d	5	6
17d	Subtract (A) - d	5	6
20dm	Load dm	10	1,6
21dm	Add (A) + dm	10	1,6
22dm	Logical product (A) and dm	10	1,6
23dm	Logical difference (A) and dm	10	1,6
24xx	Pass	5	6

TABLE 2-3. PPU INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
25xx	Pass	5	6
26xx	Pass	5	6
27xx	Pass	5	6
30d	Load (d)	15	7
31d	Add (A) + (d)	15	7
32d	Subtract (A) - (d)	15	7
33d	Logical difference (A) and (d)	15	7
34d	Store (A) at (d)	15	7
35d	Replace add (A) + (d)	25	7
36d	Replace add one (d)	25	7
37d	Replace subtract one (d)	25	7
40d	Load ((d))	15 or 25	2
41d	Add (A) + ((d))	15 or 25	2
42d	Subtract (A) - ((d))	15 or 25	2
43d	Logical difference (A) and ((d))	15 or 25	2
44d	Store (A) at ((d))	15 or 25	2
45d	Replace add (A) + ((d))	25 or 35	2
46d	Replace add one ((d))	25 or 35	2
47d	Replace subtract one ((d))	25 or 35	2
5000m	Load (m)	20	1,7
50dm	Load (m + (d))	20 or 30	1,2
5100m	Add (A) + (m)	20	1,7
51dm	Add (A) + (m + (d))	20 or 30	1,2
5200m	Subtract (A) - (m)	20	1,7

TABLE 2-3. PPU INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
52dm	Subtract (A) - (m + (d))	20 or 30	1,2
5300m	Logical difference (A) and (m)	20	1,7
53dm	Logical difference (A) and (m + (d))	20 or 30	1,2
5400m	Store (A) at (m)	20	1,7
54dm	Store (A) at (m + (d))	20 or 30	1,2
5500m	Replace add (A) + (m)	30	1,7
55dm	Replace add (A) + (m + (d))	30 or 40	1,2
5600m	Replace add one (m)	30	1,7
56dm	Replace add one (m + (d))	30 or 40	1,2
5700m	Replace subtract one (m)	30	1,7
57dm	Replace subtract one (m + (d))	30 or 40	1,2
60dm	Jump to m if channel d input word flag set	10	1,8
61dm	Jump to m if channel d input word flag not set	10	1,8
62dm	Jump to m if channel d input record flag set	10	1,8
63dm	Jump to m if channel d input record flag not set	10	1,8
64dm	Jump to m if channel d output word flag set	10	1,8
65dm	Jump to m if channel d output word flag not set	10	1,8

TABLE 2-3. PPU INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
66dm	Jump to m if channel d output record flag set	10	1,8
67dm	Jump to m if channel d output record flag not set	10	1,8
70d	Input to A from channel d	9	9
71dm	Input (A) words to m from channel d	24 or 42	1,10
72d	Output from A on channel d	9	11
73dm	Output (A) words from m on channel d	34	1,12
74d	Set output record flag on channel d	5	6
75xx	Pass	5	6
76xx	Pass	5	6
77xx	Error stop	-	-

Notes:

1. The storage reference for the second word of the current instruction word must be to the alternate bank.
2. A shorter time is obtained when full use is made of bank phasing (back-to-back storage references to alternate banks).
3. The time assumes that jump conditions are not met. If jump is met, the time is the same as for 03d instruction.
4. Designator d cannot be 00 or 77.
5. The time assumes that d equals three or less. The time increases by 1 clock period for each shift beyond three. Maximum time is 34 clock periods.
6. Storage reference(s) following the one for the current instruction word must be to alternate bank(s).

TABLE 2-3. PPU INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODEL 176 (Contd)

7. Storage reference(s) following the one for the current instruction word may be to either bank.

8. The time assumes that either jump conditions are not met or jump is taken to the alternate bank. If jump is taken to same bank, the time is 15 clock periods.

9. The time assumes that channel d input word flag is set. If not set, add time waiting for flag to set.

10. First time is for a two-word block input terminated by reducing the quantity in A to zero with the following assumptions.

    a. A count of 2 is in A.

    b. Channel d input word flag initially sets.

    c. The first data storage reference is to the alternate bank.

    d. Response time between resume pulse and setting of the input word flag is 2 clock periods.

    The second time is for a three-word block input terminated by setting the channel d input record flag with the following assumptions.

    a. Channel d input word flag initially sets.

    b. The first data storage reference is to the alternate bank.

    c. Response time between resume pulse and setting of the input word flag is 2 clock periods.

11. The time assumes that the channel d output word flag is clear. If not clear, add the time waiting for the flag to clear.

12. The time is for a three-word block output with the following assumptions.

    a. A count of 3 is in A.

    b. Channel d output word flag initially clears.

    c. The first data storage reference is to the alternate bank.

    d. The device response time from receipt of word pulse to transmission of resume pulse is 2 clock periods.

    e. A 2-clock-period delay occurs for word pulses and resume pulses between the PPU and the device.

TABLE 2-4. PPU INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODEL 176

Instruction Code	Description	Execution Time (Clock Periods)	Notes
No Operation			
00xx	Error stop	-	-
24xx	Pass	5	6
25xx	Pass	5	6
26xx	Pass	5	6
27xx	Pass	5	6
75xx	Pass	5	6
76xx	Error stop	-	6
77xx	Error stop	-	-
Data Transmission			
14d	Load d	5	6
15d	Load complement d	5	6
20dm	Load dm	10	1,6
30d	Load (d)	15	7
34d	Store (A) at (d)	15	7
40d	Load ((d))	15 or 25	2
44d	Store (A) at ((d))	15 or 25	2
5000m	Load (m)	20	1,7
50dm	Load (m + (d))	20 or 30	1,2
5400m	Store (A) at (m)	20	1,7
54dm	Store (A) at (m + (d))	20 or 30	1,2
Arithmetic			
16d	Add (A) + d	5	6
17d	Subtract (A) - d	5	6
21dm	Add (A) + dm	10	1,6
31d	Add (A) + (d)	15	7

TABLE 2-4. PPU INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODEL 176 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
32d	Subtract (A) - (d)	15	7
41d	Add (A) + ((d))	15 or 25	2
42d	Subtract (A) - ((d))	15 or 25	2
5100m	Add (A) + (m)	20	1,7
51dm	Add (A) + (m + (d))	20 or 30	1,2
5200m	Subtract (A) - (m)	20	1,7
52dm	Subtract (A) - (m + (d))	20 or 30	1,2
Shift			
10d	Shift (A) by d	6	5
Logical			
11d	Logical difference (A) and d	5	6
12d	Logical product (A) and d	5	6
13d	Selective clear (A) by d	5	6
22dm	Logical product (A) and dm	10	1,6
23dm	Logical difference (A) and dm	10	1,6
33d	Logical difference (A) and (d)	15	7
43d	Logical difference (A) and ((d))	15 or 25	2
5300m	Logical difference (A) and (m)	20	1,7
53dm	Logical difference (A) and (m + (d))	20 or 30	1,2
Replace			
35d	Replace add (A) + (d)	25	7

TABLE 2-4. PPU INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODEL 176 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
36d	Replace add one (d)	25	7
37d	Replace subtract one (d)	25	7
45d	Replace add (A) + ((d))	25 or 35	2
46d	Replace add one ((d))	25 or 35	2
47d	Replace subtract one ((d))	25 or 35	2
5500m	Place add (A) + (m)	30	1,7
55dm	Replace add (A) + (m + (d))	30 or 40	1,2
5600m	Replace add one (m)	30	1,7
56dm	Replace add one (m + (d))	30 or 40	1,2
5700m	Replace subtract one (m)	30	1,7
57dm	Replace subtract one (m + (d))	30 or 40	1,2
Branch			
0100m	Long jump to m	10 or 15	1,2
01dm	Long jump to m + (d)	15, 20, or 25	1,2
0200m	Return jump to m	15 or 20	1,2
02dm	Return jump to m + (d)	20, 25, or 30	1,2
03d	Unconditional jump d	7 or 10	2
04d	Zero jump d	5	3,4
05d	Nonzero jump d	5	3
06d	Plus jump d	5	3
07d	Minus jump d	5	3

TABLE 2-4. PPU INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODEL 176 (Contd)

Instruction Code	Description	Execution Time (Clock Periods)	Notes
CP and CM			
60dm	Jump to m if channel d input word flag set	10	1,8
61dm	Jump to m if channel d input word flag not set	10	1,8
62dm	Jump to m if channel d input record flag set	10	1,8
63dm	Jump to m if channel d input record flag not set	10	1,8
Input/Output			
64dm	Jump to m if channel d output word flag set	10	1,8
65dm	Jump to m if channel d output word flag not set	10	1,8
66dm	Jump to m if channel d output record flag set	10	1,8
67dm	Jump to m if channel d output record flag not set	10	1,8
70d	Input to A from channel d	9	9
71dm	Input (A) words to m from channel d	24 or 42	1,10
72d	Output from A on channel d	9	11
73dm	Output (A) words from m on channel d	34	1,12
74d	Set output record flag on channel d	5	6

Notes:

Refer to applicable notes at end of table 2-3.

PP INSTRUCTIONS AND EXECUTION TIMES

The PP instructions and their execution times are listed in table 2-5. The times listed in the execution time column assume that no conflicts occur. The notes refer to the notes at the end of the table. Execution times are given in 50-nanosecond minor cycles.

Table 2-6 contains the same information, except that it groups the instructions by their functions.

TABLE 2-5. PP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 THROUGH 760 AND 176

Instruction Code	Description	Execution Time (Minor Cycles)	Notes
0000	Pass	10	1
01dm	Long jump to m + (d)	40	2
02dm	Return jump to m + (d)	50	3
03d	Unconditional jump d	10	-
04d	Zero jump d	10	-
05d	Nonzero jump d	10	-
06d	Plus jump d	10	-
07d	Minus jump d	10	-
10d	Shift d	10	-
11d	Logical difference d	10	-
12d	Logical product d	10	-
13d	Selective clear d	10	-
14d	Load d	10	-
15d	Load complement d	10	-
16d	Add d	10	-
17d	Subtract d	10	-
20dm	Load dm	20	-
21dm	Add dm	20	-
22dm	Logical product dm	20	-
23dm	Logical difference dm	20	-
2400	Pass	10	-
2500	Pass	10	-
260x	Exchange jump	10	4
261x	Monitor exchange jump	10	4
262x	Monitor exchange jump to MA	10	4

TABLE 2-5. PP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 THROUGH 760 AND 176 (Contd)

Instruction Code	Description	Execution Time (Minor Cycles)	Notes
27x	Read program address	10	-
30d	Load (d)	20	-
31d	Add (d)	20	-
32d	Subtract (d)	20	-
33d	Logical difference (d)	20	-
34d	Store (d)	20	-
35d	Replace add (d)	30	-
36d	Replace add one (d)	30	-
37d	Replace subtract one (d)	30	-
40d	Load ((d))	30	-
41d	Add ((d))	30	-
42d	Subtract ((d))	30	-
43d	Logical difference ((d))	30	-
44d	Store ((d))	30	-
45d	Replace add ((d))	40	-
46d	Replace add one ((d))	40	-
47d	Replace subtract one ((d))	40	-
50dm	Load (m + (d))	40	2
51dm	Add (m + (d))	40	2
52dm	Subtract (m + (d))	40	2
53dm	Logical difference (m + (d))	40	2
54dm	Store (m + (d))	40	2
55dm	Replace add (m + (d))	50	3
56dm	Replace add one (m + (d))	50	3

TABLE 2-5. PP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 THROUGH 760 AND 176 (Contd)

Instruction Code	Description	Execution Time (Minor Cycles)	Notes
57dm	Replace subtract one (m + (d))	50	3
60d	Central read from (A) to d	80	-
61dm	Central read (d) words from (A) to m	60+50/60-bit word	5
62d	Central write to (A) from d	60	5
63dm	Central write (d) words to (A) from m	60+50/60-bit word	5
64dm	Jump to m if channel d active	20	-
65dm	Jump to m if channel d inactive	20	-
66dm	Jump to m if channel d full	20	-
67dm	Jump to m if channel d empty	20	-
70d	Input to A from channel d	20	-
71dm	Input (A) words to m from channel d	50+10/word	-
72d	Output from A on channel d	20	-
73dm	Output (A) words from m on channel d	50+10/word	-
74d	Activate channel d	20	-
75d	Disconnect channel d	20	-
76d	Function (A) on channel d	20	-
77dm	Function m on channel d	20	-

TABLE 2-5. PP INSTRUCTIONS IN NUMERIC SEQUENCE FOR MODELS 720 THROUGH 760 AND 176 (Contd)

Notes:

1. If d = 20 cycles.
2. If d = 30 cycles.
3. If d = 40 cycles.
4. Assuming no CMC access conflicts.
5. Assuming no conflicts within CMC or pyramids.

TABLE 2-6. PP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 720 THROUGH 760 AND 176

Instruction Code	Description	Execution Time (Minor Cycles)	Notes
No Operation			
0000	Pass	10	1
2400	Pass	10	-
2500	Pass	10	-
Data Transmission			
14d	Load d	10	-
15d	Load complement d	10	-
20dm	Load dm	20	-
30d	Load (d)	20	-
34d	Store d	20	-
40d	Load ((d))	30	-
44d	Store ((d))	30	-
50dm	Load (m + (d))	40	-
54dm	Store (m + (d))	40	-
Arithmetic			
16d	Add d	10	-
17d	Subtract d	10	-
21dm	Add dm	20	-
31d	Add (d)	20	-
32d	Subtract (d)	20	-
41d	Add ((d))	30	-
42d	Subtract ((d))	30	-
51dm	Add (m + (d))	40	2
52dm	Subtract (m + (d))	40	2
Shift			
10d	Shift d	10	-

TABLE 2-6. PP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 720 THROUGH 760 AND 176 (Contd)

Instruction Code	Description	Execution Time (Minor Cycles)	Notes
Logical			
11d	Logical difference d	10	-
12d	Logical product d	10	-
13d	Selective clear d	10	-
22dm	Logical product dm	20	-
23dm	Logical difference dm	20	-
33d	Logical difference (d)	20	-
43d	Logical difference ((d))	30	-
53dm	Logical difference (m + (d))	40	2
Replace			
35d	Replace add (d)	30	-
36d	Replace add one (d)	30	-
37d	Replace subtract one (d)	30	-
45d	Replace add ((d))	40	-
46d	Replace add one ((d))	40	-
47d	Replace subtract one ((d))	40	-
55dm	Replace add (m + (d))	-	3
56dm	Replace add one (m + (d))	-	3
57dm	Replace subtract one (m + (d))	-	3
Branch			
01dm	Long jump to m + (d)	40	2
02dm	Return jump to m + (d)	50	3

TABLE 2-6. PP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 720 THROUGH 760 AND 176 (Contd)

Instruction Code	Description	Execution Time (Minor Cycles)	Notes
03d	Unconditional jump d	10	-
04d	Zero jump d	10	-
05d	Nonzero jump d	10	-
06d	Plus jump d	10	-
07d	Minus jump d	10	-
CP and CM			
260x	Exchange jump	10	4
261x	Monitor exchange jump	10	4
262x	Monitor exchange jump to MA	10	4
27x	Read program address	10	-
60d	Central read from (A) to d	-	-
61dm	Central read (d) words from (A) to m	-	5
62d	Central write to (A) from d	60	5
63dm	Central write (d) words to (A) from m	60+50/word	5
Input/Output			
64dm	Jump to m if channel d active	20	-
65dm	Jump to m if channel d inactive	20	-
66dm	Jump to m if channel d full	20	-
67dm	Jump to m if channel d empty	20	-
70d	Input to A from channel d	20	-
71dm	Input (A) words to m from channel d	50+10/word	-

TABLE 2-6. PP INSTRUCTIONS IN FUNCTIONAL GROUPS FOR MODELS 720 THROUGH 760 AND 176 (Contd)

Instruction Code	Description	Execution Time (Minor Cycles)	Notes
72d	Output from A on channel d	20	-
73dm	Output (A) words from m on channel d	50+10/word	-
74d	Activate channel d	20	-
75d	Disconnect channel d	20	-
76d	Function (A) on channel d	20	-
77dm	Function m on channel d	20	-

Notes:

Refer to applicable notes at end of table 2-5.

EXTERNAL FUNCTION CODES AND STATUS RESPONSES 3

STATUS AND CONTROL REGISTER

DESCRIPTOR WORD FORMAT

The descriptor word format (figure 3-1) has 12 bits that define a word or bit address and a function code. Bits 0 through 7 contain the word or bit address that designates a 12-bit word or single bit on which the function is to be performed. Bit 8 is not used. Bits 9 through 11 contain the octal function code which tests, clears, and sets the status and control register.

The following list contains the eight function codes designated by bits 9 through 11.

Function Code	Description
0	Read word.
1	Test bit.
2	Clear bit.
3	Test/clear bit.
4	Set bit.
5	Test/set bit.
6	Clear all bits.
7	Test error bits.

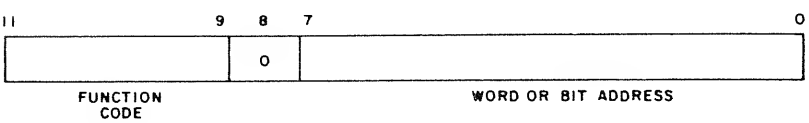

Figure 3-1. Descriptor Word Format

BIT ASSIGNMENTS

Table 3-1 lists the bit assignments for models 720 through 760. Table 3-2 lists the bit assignments for model 176. The significance of the table columns is as follows:

Column	Description
Word	Register word listed in octal.
Bit	Register bit listed in decimal and in octal.
Model	CYBER 170 models to which the bit is applicable.
S/C	S = Status bit; C = Control bit.
Function	Applicable programming functions:
	TE — Read, test, clear, test/clear, set, test/set, clear all, and test error (status bit included in test error).
	R — Read.
	D — Read, test, clear, test/clear, test, test/set, and clear all.
	Blank — Read, test, clear, test/clear, set, test/set, and clear all.
Notes	Applicable notes are at the end of the table.

The channel 36 status and control register is available for 20 PP systems and is applicable to bits indicated by note 1 in tables 3-1 and 3-2.

TABLE 3-1. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
0	0	0	CM parity error	X	X	S	TE	1
	1	1	CSU-0 address parity error	X	X	S	TE	-
	2	2	Not used	-	-	-	-	-
	3	3	SECDED error	X	X	S	TE	2
	4	4	Not used	-	-	-	-	-
	5	5	CMC parity error	X	X	S	TE	3
	6	6	Not used	-	-	-	-	-
	7	7	Not used	-	-	-	-	-
	8	10	Not used	-	-	-	-	-
	9	11	Not used	-	-	-	-	-
	10	12	Any error bit equals one	X	X	S	TE	4
	11	13	ECS transfer error	X	X	S	TE	5
1	12	14	CP-0 parity error	X	X	S	TE	1
	13	15	CP-1 parity error	X	-	S	TE	1,6
	14	16	PP-0 memory parity error	X	X	S	TE	1
	15	17	PP-1 memory parity error	X	X	S	TE	1
	16	20	PP-2 memory parity error	X	X	S	TE	1
	17	21	PP-3 memory parity error	X	X	S	TE	1

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	18	22	PP-4 memory parity error	X	X	S	TE	1
	19	23	PP-5 memory parity error	X	X	S	TE	1
	20	24	PP-6 memory parity error	X	X	S	TE	1
	21	25	PP-7 memory parity error	X	X	S	TE	1
	22	26	PP-8 memory parity error	X	X	S	TE	1
	23	27	PP-9 memory parity error	X	X	S	TE	1
2	24	30	Channel 0 parity error	X	X	S	TE	1,7
	25	31	Channel 1 parity error	X	X	S	TE	1,7
	26	32	Channel 2 parity error	X	X	S	TE	1,7
	27	33	Channel 3 parity error	X	X	S	TE	1,7
	28	34	Channel 4 parity error	X	X	S	TE	1,7
	29	35	Channel 5 parity error	X	X	S	TE	1,7
	30	36	Channel 6 parity error	X	X	S	TE	1,7
	31	37	Channel 7 parity error	X	X	S	TE	1,7
	32	40	Channel 10 parity error	X	X	S	TE	1,7
	33	41	Channel 11 parity error	X	X	S	TE	1,7
	34	42	Channel 12 parity error	X	X	S	TE	1,7

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	35	43	Channel 13 parity error	X	X	S	TE	1,7
3	36	44	Mains power failure	X	X	S	TE	8
	37	45	Shutdown imminent	X	X	S	TE	8
	38	46	Not used	-	-	-	TE	-
	39	47	Not used	-	-	-	TE	-
	40	50	Syndrome bit 0	X	X	S	R	9
	41	51	Syndrome bit 1	X	X	S	R	9
	42	52	Syndrome bit 2	X	X	S	R	9
	43	53	Syndrome bit 3	X	X	S	R	9
	44	54	Syndrome bit 4	X	X	S	R	9
	45	55	Syndrome bit 5	X	X	S	R	9
	46	56	Syndrome bit 6	X	X	S	R	9
	47	57	Syndrome bit 7	X	X	S	R	9
4	48	60	Syndrome address bit 0	X	X	S	R	10
	49	61	Syndrome address bit 1	X	X	S	R	10
	50	62	Syndrome address bit 2	X	X	S	R	10
	51	63	Syndrome address bit 16	X	X	S	R	10
	52	64	Syndrome address bit 17	X	X	S	R	10

TABLE 3-1. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	53	65	Not used	-	-	-	-	-
	54	66	Parity error port code bit 0	X	X	S	R	11
	55	67	Parity error port code bit 1	X	X	S	R	11
	56	70	Breakpoint port code bit 0	X	X	S	R	12
	57	71	Breakpoint port code bit 1	X	X	S	R	12
	58	72	Breakpoint function code bit 0	X	X	S	R	12
	59	73	Breakpoint function code bit 1	X	X	S	R	12
5	60	74	Pinput bit 0	X	X	S	R	1,13
	61	75	Pinput bit 1	X	X	S	R	1,13
	62	76	Pinput bit 2	X	X	S	R	1,13
	63	77	Pinput bit 3	X	X	S	R	1,13
	64	100	Pinput bit 4	X	X	S	R	1,13
	65	101	Pinput bit 5	X	X	S	R	1,13
	66	102	Pinput bit 6	X	X	S	R	1,13
	67	103	Pinput bit 7	X	X	S	R	1,13

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	68	104	Pinput bit 8	X	X	S	R	1,13
	69	105	Pinput bit 9	X	X	S	R	1,13
	70	106	Pinput bit 10	X	X	S	R	1,13
	71	107	Pinput bit 11	X	X	S	R	1,13
6	72	110	PP identification bit 0	X	X	S	R	1,13
	73	111	PP identification bit 1	X	X	S	R	1,13
	74	112	PP identification bit 2	X	X	S	R	1,13
	75	113	PP identification bit 3	X	X	S	R	1,13
	76	114	PPS breakpoint bit	X	X	S	-	1
	77	115	CMC breakpoint match	X	X	S	-	14
	78	116	Clear CM busy	-	-	-	-	-
	79	117	Not used	-	-	-	-	-
	80	120	Force zero parity on channels	X	X	C	D	1
	81	121	Force zero parity on PPM	X	X	C	D	1
	82	122	Not used	-	-	-	-	-
	83	123	PPS breakpoint mode select	X	X	C	D	1,13

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
7	84	124	All PPs 500-nanosecond major cycle	X	X	S	-	-
	85	125	Inhibit PPS request to CMC	X	X	C	D	1
	86	126	Narrow clock with margin	X	X	C	-	-
	87	127	Wide clock width margin	X	X	C	-	-
	88	130	Diagnostic aid	X	X	S	-	-
	89	131	Diagnostic aid	X	X	S	-	-
	90	132	Diagnostic aid	X	X	S	-	-
	91	133	Diagnostic aid	X	X	S	-	-
	92	134	Diagnostic aid	X	X	S	-	-
	93	135	Not used	-	-	-	-	-
	94	136	Stop on error	X	X	C	D	1
	95	137	Stop on PPM parity error	X	X	C	D	1,15
10	96	140	Breakpoint address bit 0	X	X	C	-	16
	97	141	Breakpoint address bit 1	X	X	C	-	16
	98	142	Breakpoint address bit 2	X	X	C	-	16
	99	143	Breakpoint address bit 3	X	X	C	-	16
	100	144	Breakpoint address bit 4	X	X	C	-	16
	101	145	Breakpoint address bit 5	X	X	C	-	16
	102	146	Breakpoint address bit 6	X	X	C	-	16

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	103	147	Breakpoint address bit 7	X	X	C	-	16
	104	150	Breakpoint address bit 8	X	X	C	-	16
	105	151	Breakpoint address bit 9	X	X	C	-	16
	106	152	Breakpoint address bit 10	X	X	C	-	16
	107	153	Breakpoint address bit 11	X	X	C	-	16
11	108	154	Breakpoint address bit 12	X	X	C	-	16
	109	155	Breakpoint address bit 13	X	X	C	-	16
	110	156	Breakpoint address bit 14	X	X	C	-	16
	111	157	Breakpoint address bit 15	X	X	C	-	16
	112	160	Breakpoint address bit 16	X	X	C	-	16
	113	161	Breakpoint address bit 17	X	X	C	-	16
	114	162	Breakpoint condition code bit 18	X	X	C	-	17
	115	163	Breakpoint condition code bit 19	X	X	C	-	17
	116	164	Breakpoint condition code bit 20	X	X	C	-	17
	117	165	Breakpoint condition code bit 21	X	X	C	-	17
	118	166	Inhibit single error report	X	X	C	-	18

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	119	167	CM read double error	X	X	S	D	1
12	120	170	PP select code bit 0	X	X	C	D	1,19
	121	171	PP select code bit 1	X	X	C	D	1,19
	122	172	PP select code bit 2	X	X	C	D	1,19
	123	173	PP select code bit 3	X	X	C	D	1,19
	124	174	PP select auto/manual mode	X	X	C	D	1,20
	125	175	Force exit on selected PP	X	X	C	D	1
	126	176	Force dead-start on selected PP	X	X	C	D	1,21
	127	177	Master clear	X	X	C	D	-
	128	200	Force zero SECDED code and parity CMC to CM	X	X	C	-	-
	129	201	Force zero address parity CMC to CM	X	X	C	-	-
	130	202	Disable address parity error	X	X	C	-	-
	131	203	Not used	-	-	-	-	-
13	132	204	Force zero parity code 0	X	X	C	-	-
	133	205	Force zero parity code 1	X	X	C	-	-

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	134	206	Not used	-	-	-	-	-
	135	207	Not used	-	-	-	-	-
	136	210	ECS transfer error code 0	X	X	S	R	22
	137	211	ECS transfer error code 1	X	X	S	R	22
	138	212	ECS transfer error code 2	X	X	S	R	22
	139	213	CMC address/ data parity error	X	X	S	R	23
	140	214	Not used	-	-	-	-	-
	141	215	Clock frequency margin 0	X	X	C	D	24
	142	216	Clock frequency margin 1	X	X	C	D	24
	143	217	Clock frequency slow/fast	X	X	C	D	24,25
14	144	220	RVM address bit 0 status	-	X	S	-	26
	145	221	RVM address bit 1 status	-	X	S	-	26
	146	222	RVM address bit 2 status	-	X	S	-	26
	147	223	RVM address bit 3 status	-	X	S	-	26
	148	224	RVM address bit 4 status	-	X	S	-	26
	149	225	RVM address bit 5 status	-	X	S	-	26

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	150	226	RVM hi/lo	-	X	S	-	27
	151	227	RVM all/one	-	X	S	-	28
	152	230	Clock margin width narrow	-	X	C	-	29
	153	231	Clock margin width wide	-	X	C	-	29
	154	232	Select hi/lo RVM	-	X	C	-	30
	155	233	Select all/ one RVM	-	X	C	-	31
15	156	234	RVM quadrant 0 select	-	X	C	-	32
	157	235	RVM quadrant 1 select	-	X	C	-	32
	158	236	RVM quadrant 2 select	-	X	C	-	32
	159	237	RVM quadrant 3 select	-	X	C	-	32
	160	240	RVM quadrant 4 select	-	X	C	-	32
	161	241	RVM quadrant 5 select	-	X	C	-	32
	162	242	RVM quadrant 6 select	-	X	C	-	32
	163	243	RVM quadrant 7 select	-	X	C	-	32
	164	244	RVM quadrant 8 select	-	X	C	-	32
	165	245	RVM quadrant 9 select	-	X	C	-	32
	166	246	RVM quadrant 10 select	-	X	C	-	32

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	167	247	RVM quadrant 11 select	-	X	C	-	32
16	168	250	RVM module address bit 0	-	X	C	-	33
	169	251	RVM module address bit 1	-	X	C	-	33
	170	252	RVM module address bit 2	-	X	C	-	33
	171	253	RVM module address bit 3	-	X	C	-	33
	172	254	RVM module address bit 4	-	X	C	-	33
	173	255	RVM module address bit 5	-	X	C	-	33
	174	256	PPS to CMC zero address parity	X	X	C	-	1
	175	257	PPS to CMC zero data parity	X	X	C	-	1
	176	260	Not used	-	-	-	-	-
	177	261	Not used	-	-	-	-	-
	178	262	Not used	-	-	-	-	-
	179	263	Not used	-	-	-	-	-
17	180	264	Not used	-	-	-	-	-
	181	265	Not used	-	-	-	-	-
	182	266	Not used	-	-	-	-	-
	183	267	Double error	X	X	S	-	-
	184	270	Not used	-	-	-	-	-
	185	271	CP-1 to CMC zero address parity	X	-	C	-	6

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	Model 720/ 730	Model 740/ 750/ 760	S/C	Function	Notes
	186	272	Not used	-	-	-	-	-
	187	273	CP-1 to CMC zero data parity	X	-	C	-	6
	188	274	Software flag 0	X	X	C	-	1,34
	189	275	Software flag 1	X	X	C	-	1,34
	190	276	Syndrome address bit 3	X	X	-	-	-
	191	277	Not used	-	-	-	-	-
20	192	300	CP-0 stopped	X	X	S	R	-
	193	301	CP-1 stopped	X	-	S	R	6
	194	302	ECS in progress flag	X	X	S	R	-
	195	303	Monitor flag CP-0	X	X	S	R	-
	196	304	Monitor flag CP-1	X	-	S	R	6
	197	305	PPM select bit 0	X	X	S	R	-
	198	306	PPM select bit 1	X	X	S	R	-
	199	307	PPM select bit 2	X	X	S	R	-
	200	310	PPM select bit 3	X	X	S	R	-
	201	311	External channel select	X	X	S	R	35
	202	312	Not used	-	-	-	-	-
	203	313	Not used	-	-	-	-	-

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

Notes:

1. The bit is also used in the abbreviated status and control register of optional PPS-1.
2. Loads and locks bits 40 through 52 and 190.
3. Loads and locks bits 054, 55, and 139.
4. Tests 0 through 39 of PPS-1.
5. Loads and locks bits 136 through 138.
6. Use only in dual-CP models.
7. For channel 36, channel numbers 20 through 33 (octal) apply.
8. Power/environmental abnormal condition.
9. Loaded and locked by bit 3 (memory SECDED error).
10. Loaded and locked by bit 3.
11. From CMC, identifies port; loaded and locked by bit 5.
12. Loaded and locked by bit 77.
13. If bit 83 clears, bits 60 through 71 display P of the PP selected by bits 120 through 123, and bits 72 through 75 display selected PP. If bit 83 sets, the content of the P register is latched and retained on every CM breakpoint bit. If bit 76 sets when bit 83 sets, bits 60 through 75 hold until bit 76 clears.
14. Loads and locks bits 56 through 59.
15. Applies to all PPs.
16. Absolute 18-bit address (bits 96 through 113 are sent to and used by CMC to establish a breakpoint address when bits 116 and/or 117 are set).
17. Select function RD/WT/RNI or all three to CMC for port selection.
18. Single errors are not recorded in SCR when set.
19. Select 1 of 10 PPs for forced exit, deadstart, or display.
20. Clear equals manual.

TABLE 3-1. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODELS 720 THROUGH 760 (Contd)

21. Set forces deadstart (PP remains in deadstart condition until bit clears).

22. Loaded and locked by bit 11.

23. Loaded and locked by bit 5. Clear equals data error.

24. Bits 141 through 143 are code bits for selecting clock margins.

25. Clear equals slow.

26. Indicates module having reference voltage margins (RVM) applied. Bits 144 through 151 apply only to models 740, 750, and 760.

27. Clear equals lo.

28. Clear equals one.

29. Bits 152 and 153 apply one to models 740, 750, and 760.

30. Clear equals lo. Bit applies only to models 740, 750, and 760.

31. Clear equals one. Bit applies only to models 740, 750, and 760.

32. Used with bits 154 and 155. Bits 156 through 167 apply only to models 740,750, and 760.

33. Bits 186 through 173 apply only to models 740, 750, and 760.

34. Diagnostic aids.

35. PPS select.

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
0	0	0	Not used	-	-	-
	1	1	Not used	-	-	-
	2	2	Not used	-	-	-
	3	3	CM rank 2 error	S	TE	-
	4	4	PPU error	S	TE	-
	5	5	Not used	-	-	-
	6	6	Not used	-	-	-
	7	7	Not used	-	-	-
	8	10	Not used	-	-	-
	9	11	Not used	-	-	-
	10	12	Any error bit equals one	S	-	2
	11	13	LCME rank 2 error	S	TE	-
1	12	14	Not used	-	-	-
	13	15	Not used	-	-	-
	14	16	PP-0 memory parity error	S	TE	1
	15	17	PP-1 memory parity error	S	TE	1
	16	20	PP-2 memory parity error	S	TE	1
	17	21	PP-3 memory parity error	S	TE	1
	18	22	PP-4 memory parity error	S	TE	1
	19	23	PP-5 memory parity error	S	TE	1
	20	24	PP-6 memory parity error	S	TE	1
	21	25	PP-7 memory parity error	S	TE	1

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
	22	26	PP-8 memory parity error	S	TE	1
	23	27	PP-9 memory parity error	S	TE	1
2	24	30	Channel 0 parity error	S	TE	1,3
	25	31	Channel 1 parity error	S	TE	1,3
	26	32	Channel 2 parity error	S	TE	1,3
	27	33	Channel 3 parity error	S	TE	1,3
	28	34	Channel 4 parity error	S	TE	1,3
	29	35	Channel 5 parity error	S	TE	1,3
	30	36	Channel 6 parity error	S	TE	1,3
	31	37	Channel 7 parity error	S	TE	1,3
	32	40	Channel 10 parity error	S	TE	1,3
	33	41	Channel 11 parity error	S	TE	1,3
	34	42	Channel 12 parity error	S	TE	1,3
	35	43	Channel 13 parity error	S	TE	1,3
3	36	44	Mains power failure	S	TE	-
	37	45	Shutdown imminent	S	TE	4
	38	46	Not used	-	-	-
	39	47	Not used	-	-	-

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
	40	50	CM syndrome bit 0	S	R	-
	41	51	CM syndrome bit 1	S	R	-
	42	52	CM syndrome bit 2	S	R	-
	43	53	CM syndrome bit 3	S	R	-
	44	54	CM syndrome bit 4	S	R	-
	45	55	CM syndrome bit 5	S	R	-
	46	56	CM syndrome bit 6	S	R	-
	47	57	CM syndrome bit 7	S	R	-
4	48	60	CM error address bit 16	S	R	-
	49	61	CM error address bit 17	S	R	-
	50	62	CM error address bit 0	S	R	-
	51	63	CM error address bit 1	S	R	-
	52	64	CM error address bit 2	S	R	-
	53	65	CM error address bit 3	S	R	-
	54	66	Exchange buffer bias bit 0	C	-	-
	55	67	Exchange buffer bias bit 1	C	-	-
	56	70	Exchange buffer bias bit 2	C	-	-
	57	71	Exchange buffer bias bit 3	C	-	-
	58	72	Deadstart PPU	C	-	-
	59	73	Deaddump PPU	C	-	-

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
5	60	74	P input bit 0	S	R	1,5
	61	75	P input bit 1	S	R	1,5
	62	76	P input bit 2	S	R	1,5
	63	77	P input bit 3	S	R	1,5
	64	100	P input bit 4	S	R	1,5
	65	101	P input bit 5	S	R	1,5
	66	102	P input bit 6	S	R	1,5
	67	103	P input bit 7	S	R	1,5
	68	104	P input bit 8	S	R	1,5
	69	105	P input bit 9	S	R	1,5
	70	106	P input bit 10	S	R	1,5
	71	107	P input bit 11	S	R	1,5
6	72	110	Scanner select bit 0	C	-	-
	73	111	Scanner select bit 1	C	-	-
	74	112	Scanner select bit 2	C	-	-
	75	113	Scanner select bit 3	C	-	-
	76	114	Block copy exit control and enable central computer master clear	-	-	6
	77	115	Deadstart CPU	C	-	-
	78	116	Not used	-	-	-
	79	117	Not used	-	-	-
	80	120	Force zero parity on channels	C	D	1
	81	121	Force zero parity on PPM	C	D	1

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
7	82	122	Enable scanner interface	C	D	-
	83	123	Clear 7000 PPU parity error	C	D	-
	84	124	All PPs 500-nanosecond major cycle	C	D	-
	85	125	Inhibit PPS request to CM	C	D	-
	86	126	Narrow clock width margin	C	-	7
	87	127	Wide clock wdith margin	C	-	7
	88	130	LCME degrade control bit 0	C	D	-
	89	131	LCME degrade control bit 1	C	D	-
	90	132	LCME degrade control bit 2	C	D	-
	91	133	Reserved for possible LCME expansion	C	-	-
	92	134	Reserved for possible LCME expansion	C	-	-
	93	135	Not used	-	-	-
	94	136	Stop on error	C	D	1
	95	137	Stop on PPM parity error	C	D	1
10	96	140	LCME error address bit 0	S	R	-
	97	141	LCME error address bit 1	S	R	-
	98	142	LCME error address bit 2	S	R	-
	99	143	LCME error address bit 3	S	R	-

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
	100	144	LCME error address bit 4	S	R	-
	101	145	LCME error address bit 5	S	R	-
	102	146	LCME error address bit 6	S	R	-
	103	147	LCME error address bit 7	S	R	-
	104	150	LCME error address bit 8	S	R	-
	105	151	LCME error address bit 9	S	R	-
	106	152	LCME error address bit 10	S	R	-
	107	153	LCME error address bit 11	S	R	-
11	108	154	LCME error address bit 12	S	R	-
	109	155	LCME error address bit 13	S	R	-
	110	156	LCME error address bit 14	S	R	-
	111	157	LCME error address bit 15	S	R	-
	112	160	LCME error address bit 16	S	R	-
	113	161	LCME error address bit 17	S	R	-
	114	162	LCME error address bit 18	S	R	-
	115	163	LCME error address bit 19	S	R	-
	116	164	LCME error address bit 20	S	R	-

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
	117	165	Reserved for possible LCME expansion	S	R	-
	118	166	Inhibit CM single-bit error reporting	C	TE	-
	119	167	CM read parity or double error	S	TE	1
12	120	170	PP select code bit 0	C	D	1,8
	121	171	PP select code bit 1	C	D	1,8
	122	172	PP select code bit 2	C	D	1,8
	123	173	PP select code bit 3	C	D	1,8
	124	174	PP select auto/manual mode	C	D	1,9
	125	175	Force exit on selected PP	C	D	1
	126	176	Force PP deadstart on selected PP	C	D	1,10
	127	177	CPU clear I/O	C	D	-
	128	200	CM configuration status bit 0	S	R	-
	129	201	CM configuration status bit 1	S	R	-
	130	202	CM configuration status bit 2	S	R	-
	131	203	CM configuration status bit 3	S	R	-
13	132	204	PPU parity error stack 0	S	R	-
	133	205	PPU parity error stack 1	S	R	-
	134	206	PPU parity error stack 2	S	R	-
	135	207	PPU parity error stack 3	S	R	-

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
	136	210	PPU program error	S	R	-
	137	211	PPU stop enable	C	-	-
	138	212	CPU enable	C	-	-
	139	213	Not used	-	-	-
	140	214	CM test mode	C	-	-
	141	215	Clock frequency margins fast	C	-	-
	142	216	Clock frequency margins slow	C	-	-
	143	217	7000 clock margin condition	S	R	-
14	144	220	LCME syndrome bit 0	S	R	-
	145	221	LCME syndrome bit 1	S	R	-
	146	222	LCME syndrome bit 2	S	R	-
	147	223	LCME syndrome bit 3	S	R	-
	148	224	LCME syndrome bit 4	S	R	-
	149	225	LCME syndrome bit 5	S	R	-
	150	226	LCME syndrome bit 6	S	R	-
	151	227	LCME syndrome bit 7	S	R	-
	152	230	Narrow clock pulse width	C	-	-
	153	231	Wide clock pulse width	C	-	-
	154	232	RVM hi/lo select	C	-	11
	155	233	RVM all/one select	C	-	12

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
15	156	234	CM error address bit 4	S	R	-
	157	235	CM error address bit 5	S	R	-
	158	236	CM error address bit 6	S	R	-
	159	237	CM error address bit 7	S	R	-
	160	240	CM error address bit 8	S	R	-
	161	241	CM error address bit 9	S	R	-
	162	242	CM error address bit 10	S	R	-
	163	243	CM error address bit 11	S	R	-
	164	244	CM error address bit 12	S	R	-
	165	245	CM error address bit 13	S	R	-
	166	246	CM error address bit 14	S	R	-
	167	247	CM error address bit 15	S	R	-
16	168	250	CM clear rank 2 error	C	-	-
	169	251	CM clear rank 1 error	C	-	-
	170	252	LCME half-zero test	C	-	-
	171	253	LCME parity mode	C	-	-
	172	254	LCME maintenance mode	C	-	-
	173	255	LCME test mode	C	-	-
	174	256	CM parity mode	C	-	-

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
	175	257	CM maintenance mode	C	-	-
	176	260	Clear LCME rank 2 error	C	-	-
	177	261	Clear LCME rank 1 error	C	-	-
	178	262	Inhibit LCME single-bit error reporting	C	-	-
	179	263	Channels 2 and 3 buffer bias bit 0	C	-	-
17	180	264	Channels 2 and 3 buffer bias bit 1	C	-	-
	181	265	Channels 2 and 3 buffer bias bit 2	C	-	-
	182	266	Channels 2 and 3 buffer bias bit 3	C	-	-
	183	267	CM SECDED double-bit error	S	R	-
	184	270	Channels 4 through 7 buffer bias bit 0	C	-	-
	185	271	Channels 4 through 7 buffer bias bit 1	C	-	-
	186	272	Channels 4 through 7 buffer bias bit 2	C	-	-
	187	273	Channels 4 through 7 7 buffer bias bit 3	C	-	-
	188	274	Software lock test	C	-	-
	189	275	Software lock clear	C	-	-
	190	276	Reserved for future LCME degrade	S	-	-
	191	277	Reserved for future LCME degrade	S	-	-
20	192	300	LCME degrade status bit 0	S	R	-

TABLE 3-2. STATUS AND CONTROL REGISTER BIT ASSIGNMENTS FOR MODEL 176 (Contd)

Word (8)	Bit No. (10)	Bit No. (8)	Description	S/C	Function	Notes
	193	301	LCME degrade status bit 1	S	R	-
	194	302	LCME degrade status bit 2	S	R	-
	195	303	LCME degrade status bit 3	S	R	-
	196	304	LCME SECDED double-bit error	S	R	-
	197	305	PPM select bit 0	S	R	13
	198	306	PPM select bit 1	S	R	13
	199	307	PPM select bit 2	S	R	13
	200	310	PPM select bit 3	S	R	13
	201	311	External channel select	S	R	13
	202	312	Not used	-	-	-
	203	313	Not used	-	-	-

Notes:

1. The bit is also used in the abbreviated status and control register of optional PPS-1.
2. Any of status bits 0 through 39 is set in PPS-1.
3. For channel 36, channel numbers 20 through 33 (octal) apply.
4. Power/environmental abnormal condition.
5. If bit 124 is clear, bits 60 through 71 display the P register of PP selected by external switches. If bit 124 is set, bits 60 through 71 display the P register of the PP selected by bits 120 through 123.
6. When bit 76 is clear, bit 77 is cleared at deadstart. When bit 76 is set, bit 77 is not cleared at deadstart.

TABLE 3-2. STATUS AND CONTROL REGISTER
BIT ASSIGNMENTS FOR MODEL 176 (Contd)

7.	Select 1 of 10 PPs for forced exit, deadstart, or display.
8.	Clear = manual.
9.	One-shot operation.
10.	Set forces deadstart. PP remains in deadstart condition until bit clears.
11.	Clear = lo.
12.	Clear = one.
13.	Indicates PPS configuration selected at deadstart panel.

DISPLAY STATION CC545

KEYBOARD

A PP must transmit a one-word function code (7020_8) to request data from the keyboard of the display station. The code prepares the display controller for an input operation. The PP then checks for an active channel and receives one character from the keyboard. This character is entered as the lower 6 bits of the word. The upper bits are cleared. There is no status report by the keyboard. Table 3-3 lists the keyboard character codes.

DATA DISPLAY

The data display can be alphanumeric (character mode) or graphic (dot mode).

Character Mode

Large, medium, and small characters are provided; 16, 32, and 64 characters per line, respectively. Table 3-3 lists the display character codes.

Dot Mode

Display dots are positioned by X and Y coordinates. The X coordinates position dots horizontally; Y coordinates position dots vertically and unblank the CRT for each dot.

Codes

A single function word is transmitted to select the presentation, mode, and character size (character mode only). Figure 3-2 illustrates the function word format. The word following the function word specifies the starting coordinates for the display (for either mode). Figure 3-3 illustrates the coordinate data word. In character mode, the subsequent words are display character codes. Figure 3-4 illustrates the character data word.

TABLE 3-3. DISPLAY STATION CHARACTER CODES

6-Bit Octal Code	Display Character	Keyboard Input
00	Space	No data
01	A	A
02	B	B
03	C	C
04	D	D
05	E	E
06	F	F
07	G	G
10	H	H
11	I	I
12	J	J
13	K	K
14	L	L
15	M	M
16	N	N
17	O	O
20	P	P
21	Q	Q
22	R	R
23	S	S
24	T	T
25	U	U
26	V	V
27	W	W
30	X	X
31	Y	Y
32	Z	Z
33	0	0
34	1	1
35	2	2
36	3	3
37	4	4
40	5	5
41	6	6
42	7	7
43	8	8

TABLE 3-3. DISPLAY STATION CHARACTER CODES (Contd)

6-Bit Octal Code	Display Character	Keyboard Input
44	9	9
45	+	+
46	-	-
47	*	*
50	/	/
51	(	(
52	)	)
53	Not used	Clear (note 1)
54	=	=
55	Not used	Not used (note 2)
56	, (comma)	, (comma)
57	. (period)	. (period)
60	Not used	CR (carriage return)
61	Not used	BKSP (backspace)
62	Not used	Space (space bar)

Notes:

1. Eleventh key on top row.
2. Thirteenth key on top row.

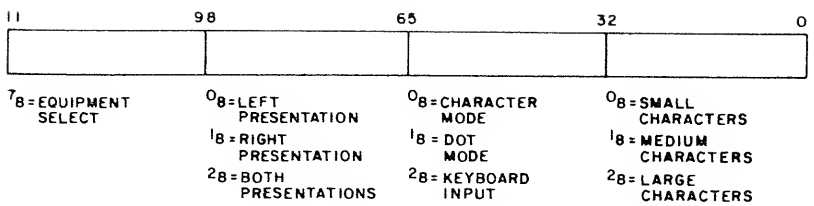

Figure 3-2. Display Station Function Word Format

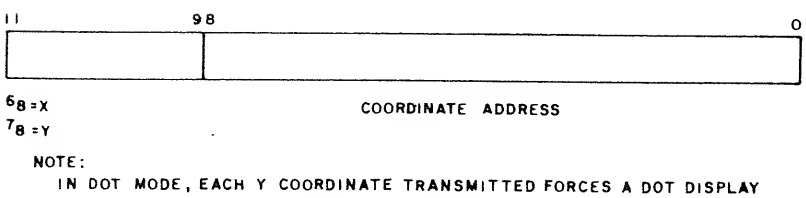

Figure 3-3. Display Station Coordinate Data Word

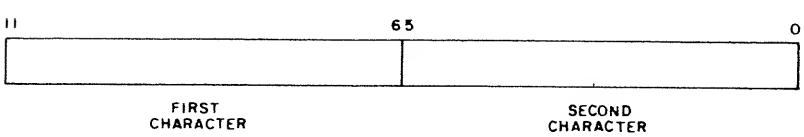

Figure 3-4. Display Station Character Data Word

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